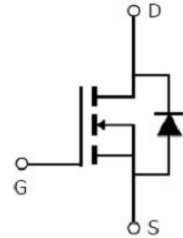


Main Product Characteristics

V_{DSS}	60V
$R_{DS(on)}$	17m Ω (typ.)
I_D	50A



TO-220



Schematic Diagram

Features and Benefits

- Advanced Process Technology
- Ideal for PWM, load switching and general purpose applications
- Ultra low on-resistance with low gate charge
- Fast switching and reverse body recovery
- 150 °C operating temperature



Description

These N-Channel enhancement mode power field effect transistors are produced using advanced MOSFET technology to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are ideal for high efficiency switch mode power supplies.

Absolute Max Ratings ($T_A=25^{\circ}C$ unless otherwise specified)

Symbol	Parameter	Max.	Units
$I_D @ T_C = 25^{\circ}C$	Continuous Drain Current, $V_{GS} @ 10V$ ①	50	A
$I_D @ T_C = 100^{\circ}C$	Continuous Drain Current, $V_{GS} @ 10V$ ①	35	
I_{DM}	Pulsed Drain Current②	200	
$P_D @ T_C = 25^{\circ}C$	Power Dissipation③	130	W
	Linear Derating Factor	1.0	W/°C
V_{DS}	Drain-Source Voltage	60	V
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy @ $L=0.3mH$	317.4	mJ
I_{AS}	Avalanche Current @ $L=0.3mH$	46	A
$T_J T_{STG}$	Operating Junction and Storage Temperature Range	-55 to + 150	°C

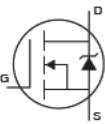
Thermal Resistance

Symbol	Characteristics	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ^③	—	1.15	°C/W
$R_{\theta JA}$	Junction-to-Ambient ($t \leq 10s$) ^④	—	62	°C/W
	Junction-to-Ambient (PCB mounted, steady-state) ^④	—	40	°C/W

Electrical Characteristics ($T_A=25^\circ\text{C}$ unless otherwise specified)

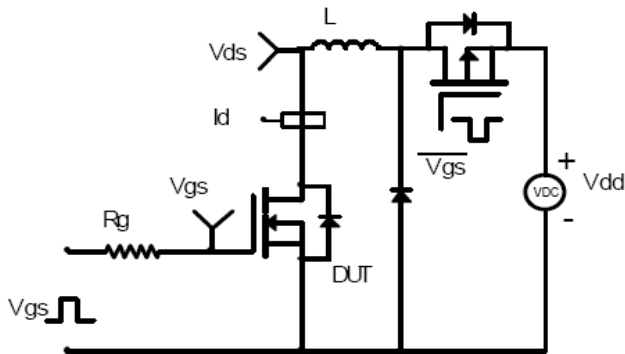
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	60	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$R_{DS(on)}$	Static Drain-to-Source On-resistance	—	17	22	m Ω	$V_{GS}=10V, I_D = 25A$
		—	30	—		$T_J = 125^\circ\text{C}$
$V_{GS(th)}$	Gate Threshold Voltage	2	—	4	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
		—	2.1	—		$T_J = 125^\circ\text{C}$
I_{DSS}	Drain-to-Source Leakage Current	—	—	1	μA	$V_{DS} = 60V, V_{GS} = 0V$
		—	—	50		$T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20V$
		—	—	-100		$V_{GS} = -20V$
Q_g	Total Gate Charge	—	23	—	nC	$I_D = 50A,$ $V_{DS}=48V,$ $V_{GS} = 10V$
Q_{gs}	Gate-to-Source Charge	—	7.9	—		
Q_{gd}	Gate-to-Drain("Miller") Charge	—	6.4	—		
$t_{d(on)}$	Turn-on Delay Time	—	28	—	ns	$V_{GS}=10V, V_{DD}=30V,$ $R_L=1.2\Omega,$ $R_{GEN}=51\Omega$ $I_D=25A$
t_r	Rise Time	—	82	—		
$t_{d(off)}$	Turn-Off Delay Time	—	108	—		
t_f	Fall Time	—	74	—		
C_{iss}	Input Capacitance	—	1630	—	pF	$V_{GS} = 0V$ $V_{DS} = 50V$ $f = 1\text{MHz}$
C_{oss}	Output Capacitance	—	235	—		
C_{rss}	Reverse Transfer Capacitance	—	34	—		

Source-Drain Ratings and Characteristics

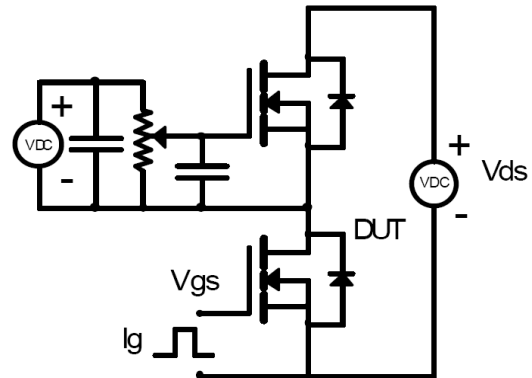
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	50	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode)	—	—	200	A	
V_{SD}	Diode Forward Voltage	—	0.85	1.5	V	$I_S=50A, V_{GS}=0V, T_J = 25^\circ\text{C}$
t_{rr}	Reverse Recovery Time	—	26.6	—	ns	$T_J = 25^\circ\text{C}, I_F = 50A,$
Q_{rr}	Reverse Recovery Charge	—	27.8	—	nC	$di/dt = 100A/\mu s$

Test Circuits and Waveforms

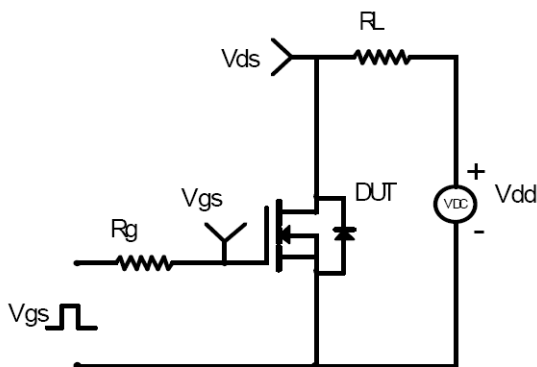
EAS Test Circuit



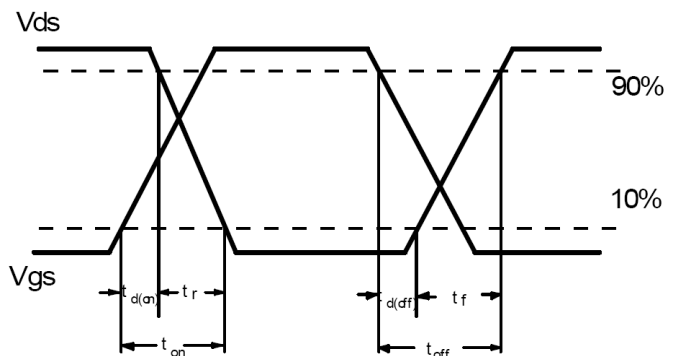
Gate charge test circuit



Switching Time Test Circuit



Switching Waveforms



Notes:

- ① The maximum current rating is limited by bond-wires.
- ② Repetitive rating; pulse width limited by max. junction temperature.
- ③ The power dissipation P_D is based on max. junction temperature, using junction-to-case thermal resistance.
- ④ The value of $R_{\theta JA}$ is measured with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with $T_A = 25^\circ\text{C}$.

Typical Electrical and Thermal Characteristics

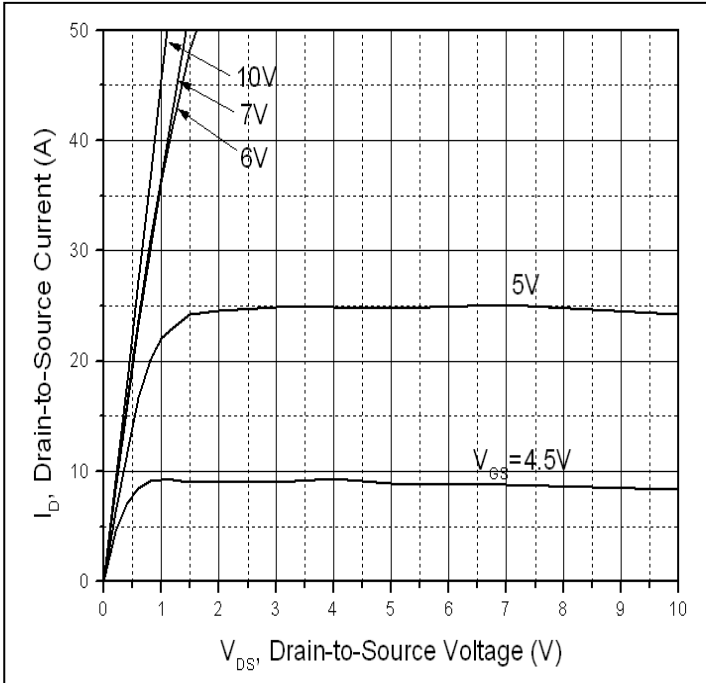


Figure 1: Typical Output Characteristics

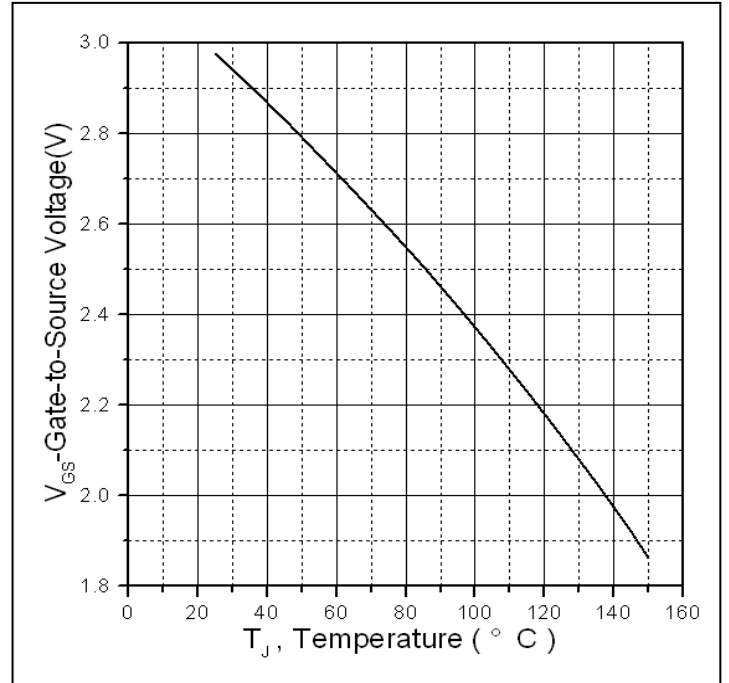


Figure 2. Gate to source cut-off voltage

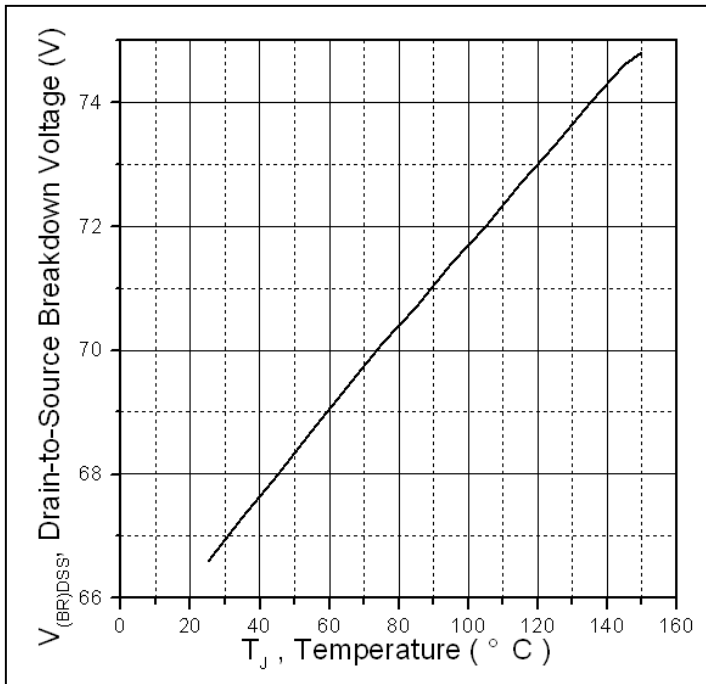


Figure 3. Drain-to-Source Breakdown Voltage vs. Temperature

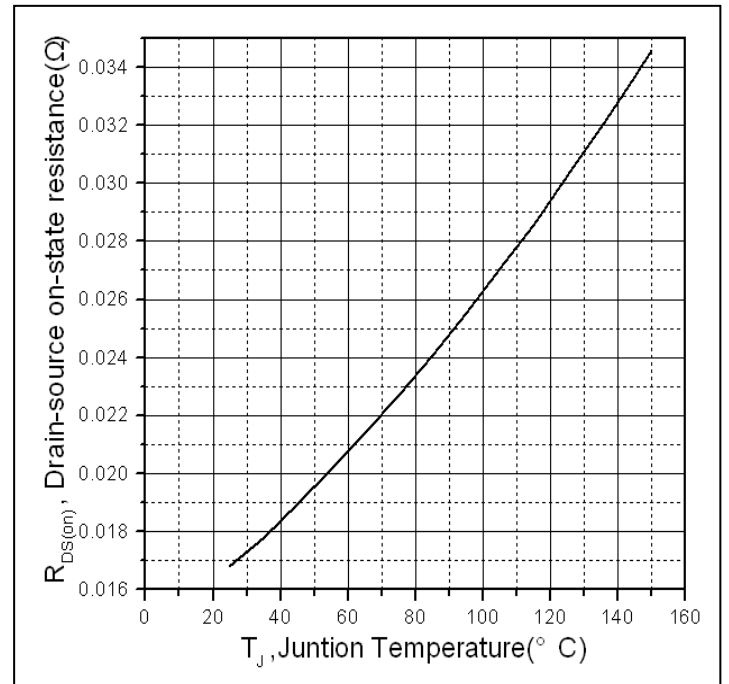


Figure 4: Normalized On-Resistance Vs. Case Temperature

Typical Electrical and Thermal Characteristics

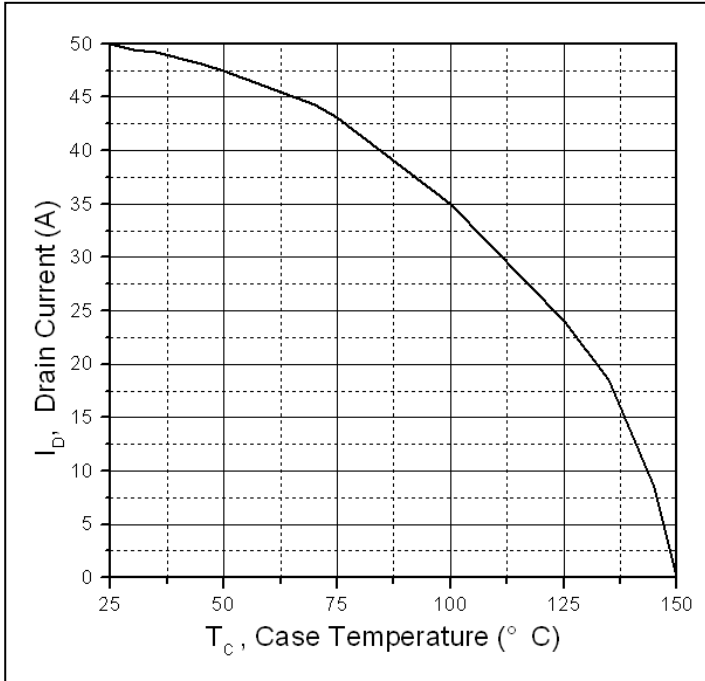


Figure 5. Maximum Drain Current Vs. Case Temperature

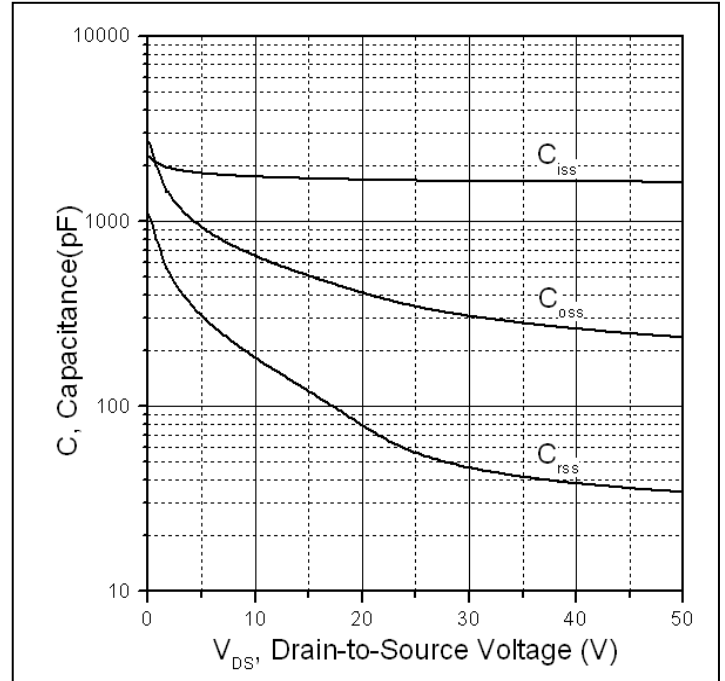
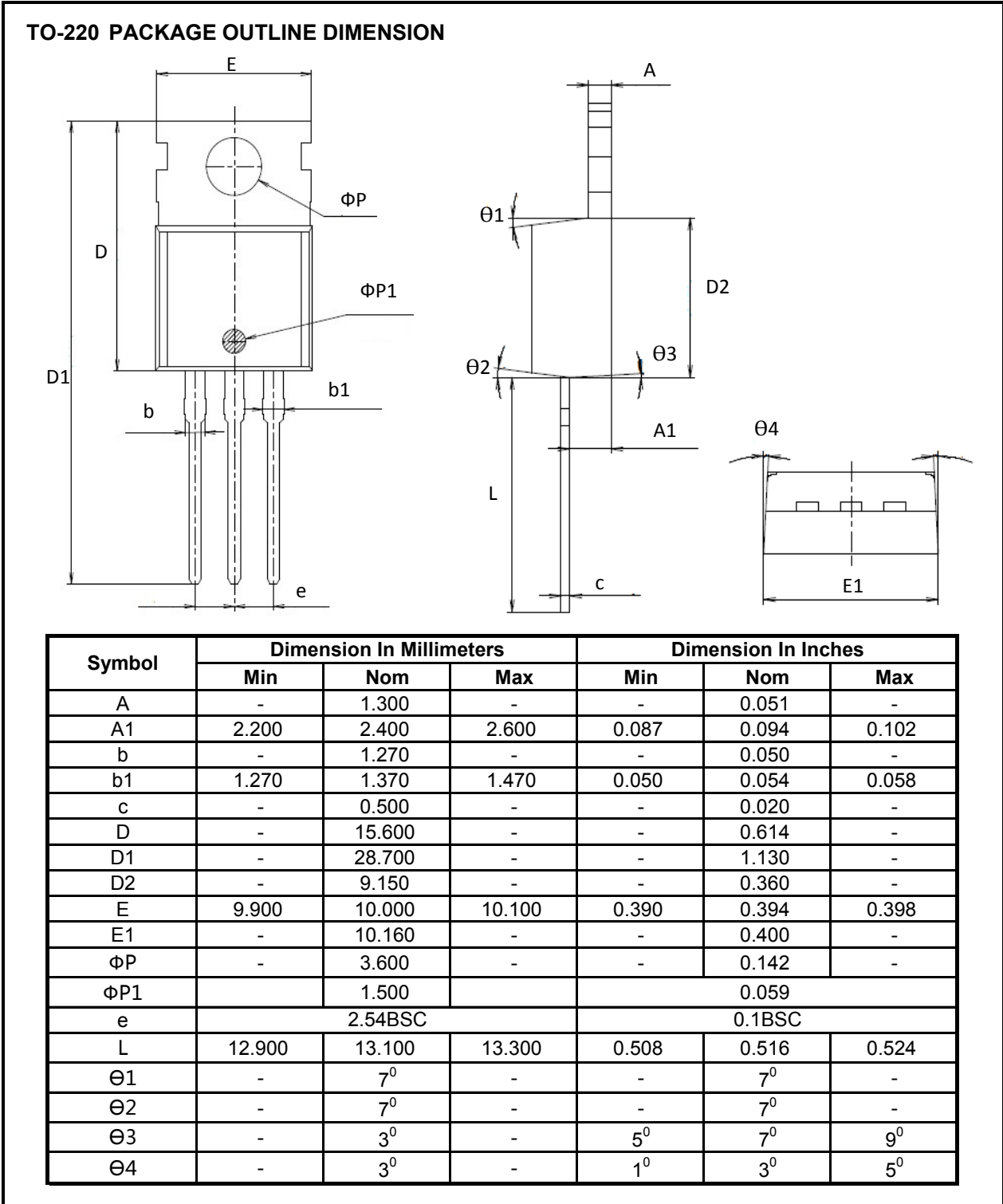


Figure 6. Typical Capacitance Vs. Drain-to-Source Voltage

Mechanical Data



Ordering and Marking Information

Device Marking: SSPL6123

Package (Available)
 TO-220
 Operating Temperature Range
 C : -55 to150 °C

Devices Per Unit

Package Type	Units/ Tube	Tubes/Inner Box	Units/Inner Box	Inner Boxes/Carton Box	Units/Carton Box
TO-220	50	20	1000	6	6000

Reliability Test Program

Test Item	Conditions	Duration	Sample Size
High Temperature Reverse Bias(HTRB)	$T_j=150^{\circ}\text{C}$ @ 80% of Max $V_{DSS}/V_{CES}/V_R$	168 hours 500 hours 1000 hours	3 lots x 77 devices
High Temperature Gate Bias(HTGB)	$T_j=150^{\circ}\text{C}$ @ 100% of Max V_{GSS}	168 hours 500 hours 1000 hours	3 lots x 77 devices