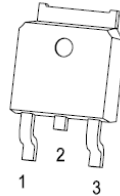


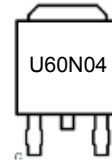
Main Product Characteristics

V_{DS}	40V
$R_{DS(on)}$	13mΩ@10V
I_D	60A

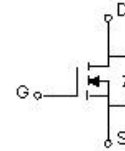
1. GATE
 2. DRAIN
 3. SOUR



TO-252 (DPAK)



Marking



Schematic Diagram

Features and Benefits

- High density cell design for ultra low $R_{DS(ON)}$
- Fully characterized Avalanche voltage and current
- Excellent stability and uniformity
- Excellent heat dissipation capability



Description

SSFU60N04 utilize the latest techniques to achieve high cell density, low on-resistance and high repetitive avalanche rating. These features make this device extremely efficient and reliable for use in power switching applications and a wide variety of other applications.

Maximum Ratings ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	40	V
Gate-Source Voltage	V_{GS}	±20	V
Continuous Drain Current	I_D	60	A
Pulsed Drain Current	I_{DM}	240	A
Single Pulsed Avalanche Energy	$E_{AS}^{(1)}$	400	mJ
Power Dissipation	P_D	1.25	W
Thermal Resistance from Junction to Ambient	$R_{\theta JA}$	100	$^\circ\text{C}/\text{W}$
Junction Temperature	T_J	150	$^\circ\text{C}$
Storage Temperature Range	T_{STG}	-55 to +150	$^\circ\text{C}$
Lead Temperature for Soldering Purposes(1/8" from case for 10s)	T_L	260	$^\circ\text{C}$

(1). E_{AS} condition: $V_{DD}=20\text{V}$, $L=0.5\text{mH}$, $R_G=25\Omega$, Starting $T_J = 25^\circ\text{C}$

Electrical Characteristics ($T_A=25^\circ\text{C}$ unless otherwise specified)

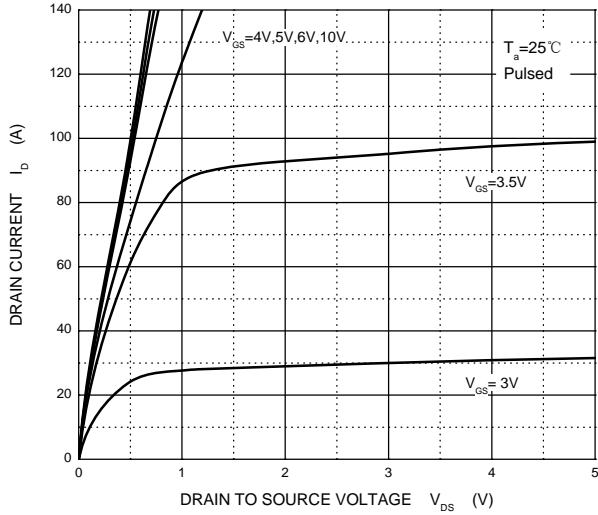
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Off characteristics						
Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	40			V
Zero gate voltage drain current	I_{DSS}	$V_{DS} = 40V, V_{GS} = 0V$			1	μA
Gate-body leakage current	I_{GSS}	$V_{DS} = 0V, V_{GS} = \pm 20V$			± 100	nA
On characteristics (note1)						
Gate-threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$	1.2	1.5	2.5	V
Static drain-source on-state resistance	$R_{DS(on)}$	$V_{GS} = 10V, I_D = 20A$		8	13	$m\Omega$
		$V_{GS} = 4.5V, I_D = 20A$		10.5	20	$m\Omega$
Forward transconductance	g_{fs}	$V_{DS} = 10V, I_D = 20A$	15			S
Dynamic characteristics (note 2)						
Input capacitance	C_{iss}	$V_{DS} = 20V, V_{GS} = 0V,$ $f = 1MHz$		1800		pF
Output capacitance	C_{oss}			280		
Reverse transfer capacitance	C_{rss}			190		
Switching characteristics (note 2)						
Total gate charge	Q_g	$V_{DS} = 20V, V_{GS} = 10V,$ $I_D = 20A$		29		nC
Gate-source charge	Q_{gs}			4.5		
Gate-drain charge	Q_{gd}			6.4		
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 20V, I_D = 2A,$ $V_{GS} = 10V, R_G = 3\Omega,$ $R_L = 1\Omega$		6.4		ns
Turn-on rise time	t_r			17.2		
Turn-off delay time	$t_{d(off)}$			29.6		
Turn-off fall time	t_f			16.8		
Drain-Source Diode Characteristics						
Drain-source diode forward voltage(note1)	V_{SD}	$V_{GS} = 0V, I_S = 20A$			1.2	V
Continuous drain-source diode forward current	I_S				60	A
Pulsed drain-source diode forward current	I_{SM}				240	A

Notes:

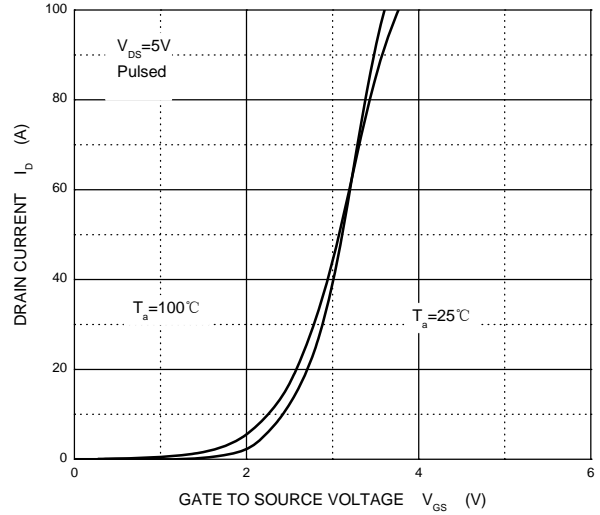
1. Pulse Test : Pulse Width $\leq 300\mu s$, duty cycle $\leq 2\%$.
2. Guaranteed by design, not subject to production.

Typical Electrical and Thermal Characteristics

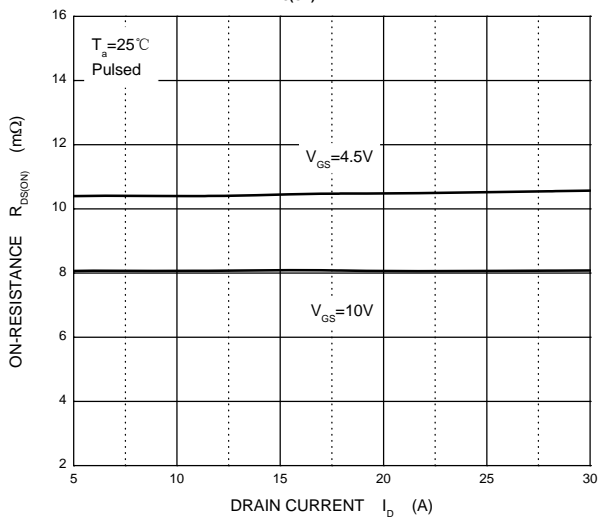
Output Characteristics



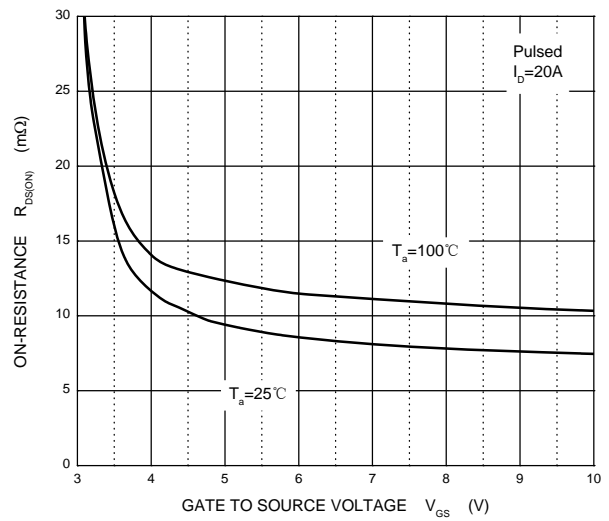
Transfer Characteristics



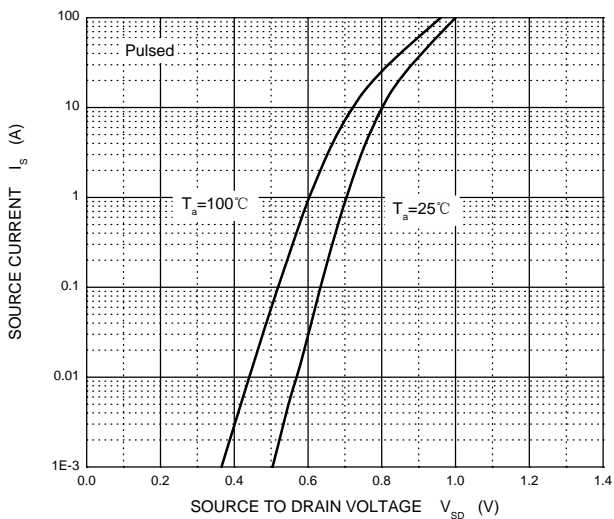
$R_{DS(ON)}$ — I_D



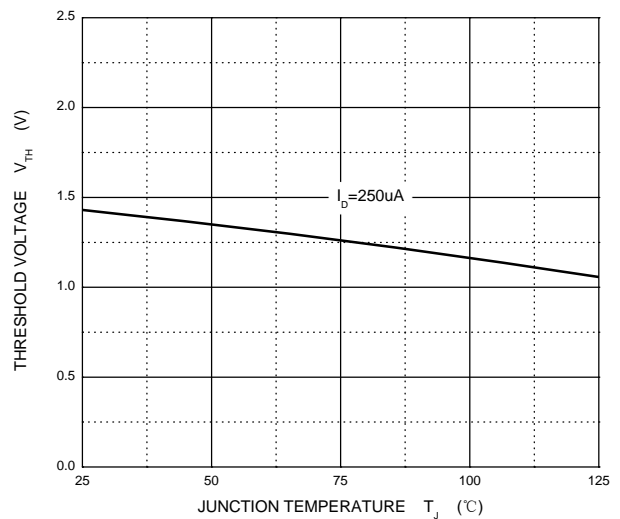
$R_{DS(ON)}$ — V_{GS}



I_S — V_{SD}

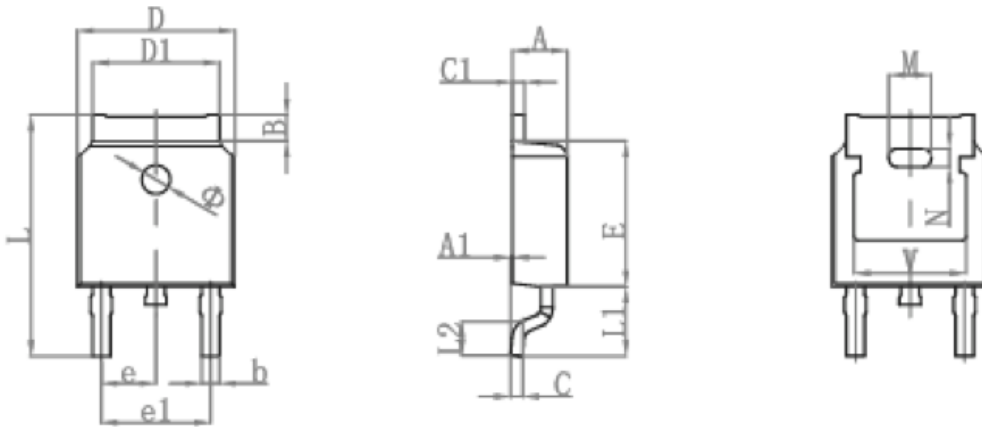


Threshold Voltage



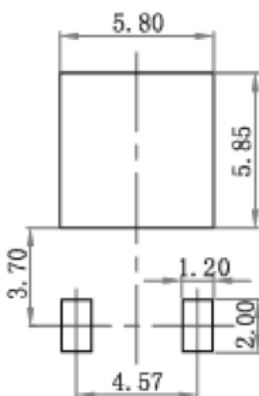
Package Outline Dimensions

TO-252 (DPAK)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	2.200	2.380	0.087	0.094
A1	0.000	0.100	0.000	0.004
B	0.800	1.400	0.031	0.055
b	0.710	0.810	0.028	0.032
c	0.460	0.560	0.018	0.022
c1	0.460	0.560	0.018	0.022
D	6.500	6.700	0.256	0.264
D1	5.130	5.460	0.202	0.215
E	6.000	6.200	0.236	0.244
e	2.286 TYP.		0.090 TYP.	
e1	4.327	4.727	0.170	0.186
M	1.778REF.		0.070REF.	
N	0.762REF.		0.018REF.	
L	9.800	10.400	0.386	0.409
L1	2.9REF.		0.114REF.	
L2	1.400	1.700	0.055	0.067
V	4.830 REF.		0.190 REF.	
Φ	1.100	1.300	0.043	0.051

Suggested Pad Layout



Note:
 1. Controlling dimension: in millimeters.
 2. General tolerance: $\pm 0.05\text{mm}$.
 3. The pad layout is for reference purposes only.