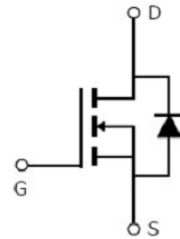


### Main Product Characteristics

$V_{DSS}$	40V
$R_{DS(on)}$	2.4m $\Omega$ (Typ.)
$I_D$	200A <sup>①</sup>



TO-220



Schematic Diagram

### Features and Benefits

- Advanced MOSFET process technology
- Ideal for PWM, load switching and general purpose applications
- Ultra low on-resistance with low gate charge
- Fast switching and reverse body recovery
- 175°C operating temperature
- Lead free



### Description

The SSFT4003 utilizes the latest processing techniques to achieve high cell density, low on-resistance and high repetitive avalanche rating. These features make this device extremely efficient and reliable for use in power switching applications and a wide variety of other applications.

### Absolute Max Ratings

Symbol	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	200 <sup>①</sup>	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	135 <sup>①</sup>	
$I_{DM}$	Pulsed Drain Current <sup>②</sup>	750	
$P_D @ T_C = 25^\circ C$	Power Dissipation <sup>③</sup>	220	W
	Linear Derating Factor	1.5	W/ $^\circ C$
$V_{DS}$	Drain-Source Voltage	40	V
$V_{GS}$	Gate-to-Source Voltage	$\pm 24$	V
$E_{AS}$	Single Pulse Avalanche Energy @ L=0.3mH	912	mJ
$I_{AS}$	Avalanche Current @ L=0.3mH	78	A
$T_J, T_{STG}$	Operating Junction and Storage Temperature Range	-55 to +175	$^\circ C$


## Thermal Resistance

Symbol	Characteristics	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case <sup>③</sup>	—	0.62	°C/W
$R_{\theta JA}$	Junction-to-Ambient ( $t \leq 10s$ ) <sup>④</sup>	—	60	°C/W
	Junction-to-Ambient (PCB mounted, steady-state) <sup>④</sup>	—	40	°C/W

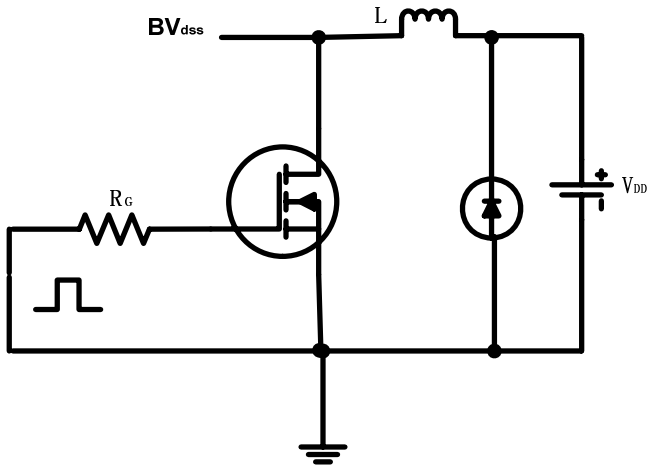
## Electrical Characteristics ( $T_A=25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	40	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$R_{DS(on)}$	Static Drain-to-Source On-resistance	—	2.4	3.5	mΩ	$V_{GS}=10V, I_D = 30A$ $T_J = 125^\circ\text{C}$
		—	4.1	—		
$V_{GS(th)}$	Gate Threshold Voltage	2	—	4	V	$V_{DS} = V_{GS}, I_D = 250\mu A$ $T_J = 125^\circ\text{C}$
		—	2.0	—		
$I_{DSS}$	Drain-to-Source Leakage Current	—	—	1	μA	$V_{DS} = 40V, V_{GS} = 0V$ $T_J = 125^\circ\text{C}$
		—	—	50		
$I_{GSS}$	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 24V$
		—	—	-100		$V_{GS} = -24V$
$Q_g$	Total Gate Charge	—	104	—	nC	$I_D = 75A,$ $V_{DS} 32V,$ $V_{GS} = 10V$
$Q_{gs}$	Gate-to-Source Charge	—	16	—		
$Q_{gd}$	Gate-to-Drain("Miller") Charge	—	40	—		
$t_{d(on)}$	Turn-on Delay Time	—	21.4	—	ns	$V_{GS}=10V, V_{DS} = 20V,$ $R_L=0.26\Omega,$ $R_{GEN}=3.0\Omega,$ $I_D = 75A$
$t_r$	Rise time	—	57.8	—		
$t_{d(off)}$	Turn-Off Delay Time	—	48.7	—		
$t_f$	Fall Time	—	19.9	—		
$C_{iss}$	Input Capacitance	—	7615	—	pF	$V_{GS} = 0V,$ $V_{DS} = 25V,$ $f = 1\text{MHz}$
$C_{oss}$	Output Capacitance	—	959	—		
$C_{rss}$	Reverse Transfer Capacitance	—	342	—		

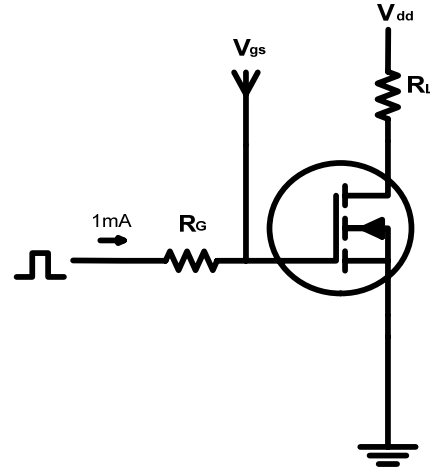
## Source-Drain Ratings and Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_S$	Continuous Source Current (Body Diode)	—	—	200 <sup>①</sup>	A	MOSFET symbol showing the integral reverse p-n junction diode. 
$I_{SM}$	Pulsed Source Current (Body Diode)	—	—	750	A	
$V_{SD}$	Diode Forward Voltage	—	0.86	1.3	V	$I_S=30A, V_{GS}=0V$
$t_{rr}$	Reverse Recovery Time	—	29.6	—	ns	$T_J = 25^\circ\text{C}, I_F = 50A, di/dt = 100A/\mu s$
$Q_{rr}$	Reverse Recovery Charge	—	22.2	—	nC	

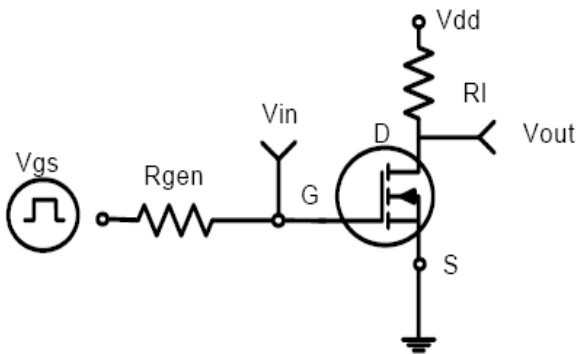
## Test Circuits and Waveforms



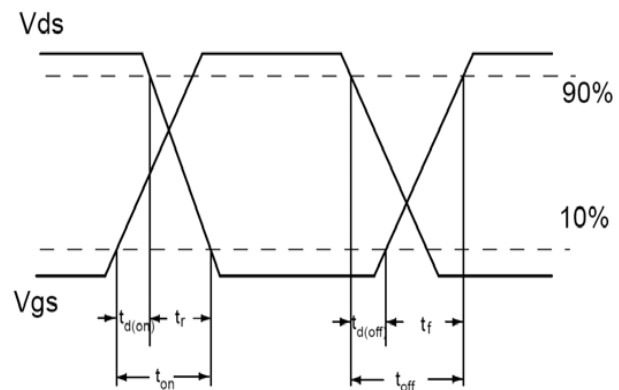
**E<sub>AS</sub> Test Circuit**



**Gate Charge Test Circuit**



**Switching Time Test Circuit**

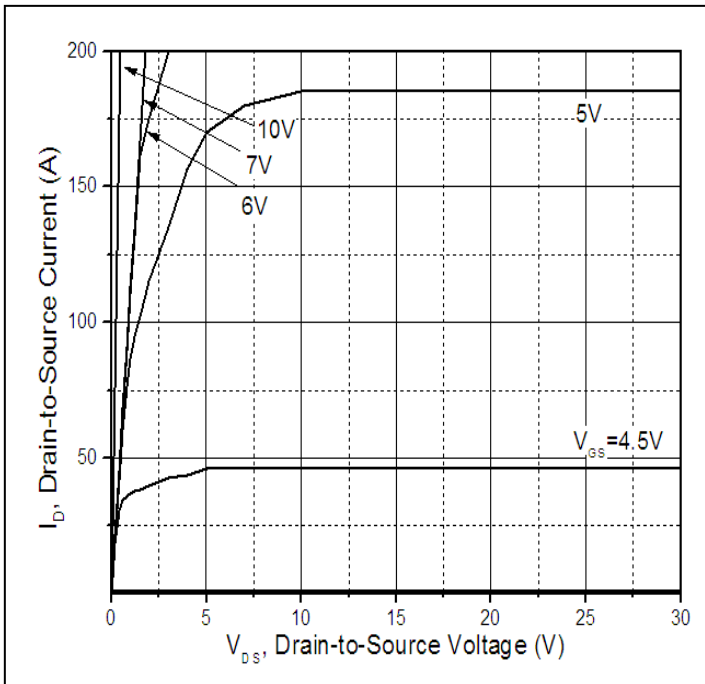


**Switching Waveform**

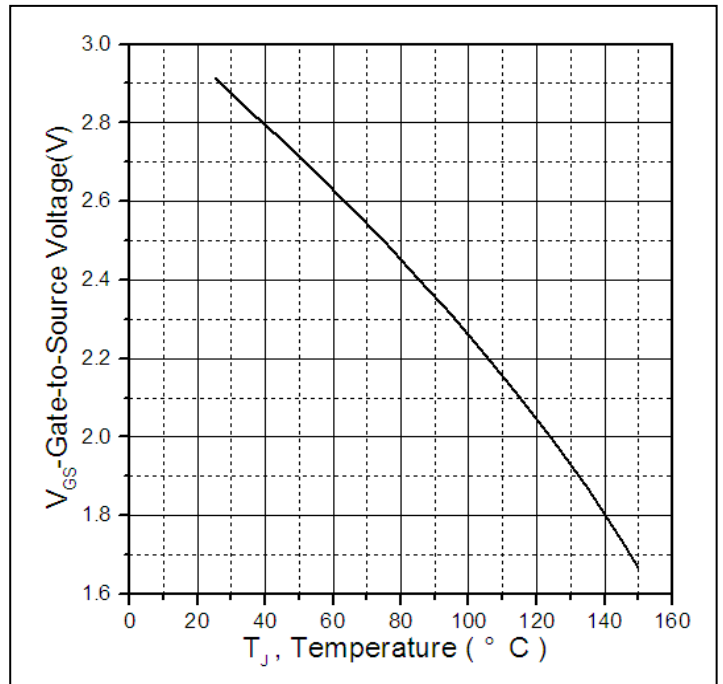
### Notes:

- ① Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 75A.
- ② Repetitive rating; pulse width limited by max junction temperature.
- ③ The power dissipation  $P_D$  is based on max junction temperature, using junction-to-case thermal resistance.
- ④ The value of  $R_{\theta JA}$  is measured with the device mounted on 1 in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with  $T_A = 25^\circ\text{C}$

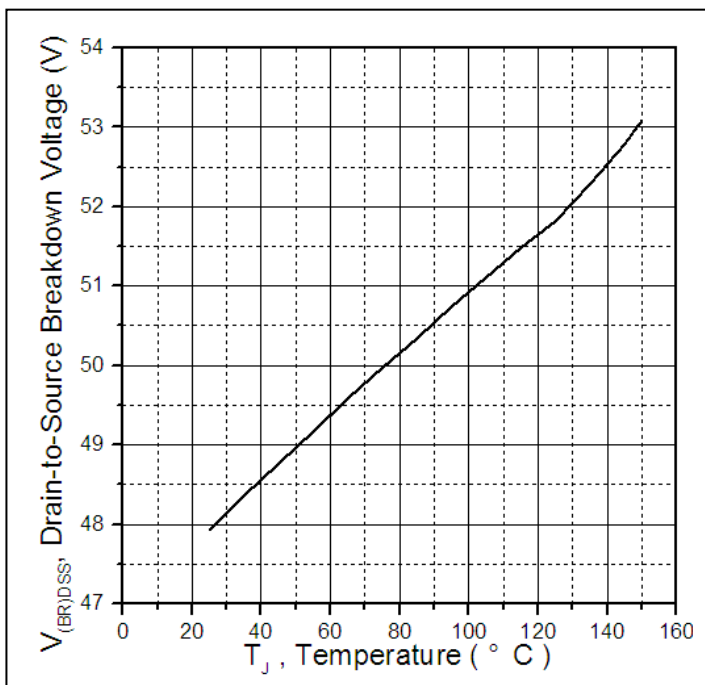
**Typical Electrical and Thermal Characteristics**



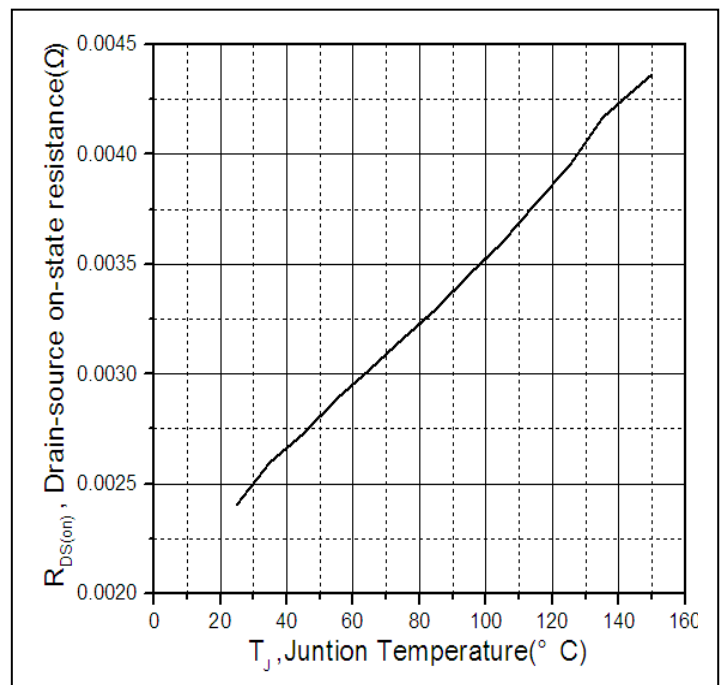
**Figure 1. Typical Output Characteristics**



**Figure 2. Gate to Source Cut-off Voltage**

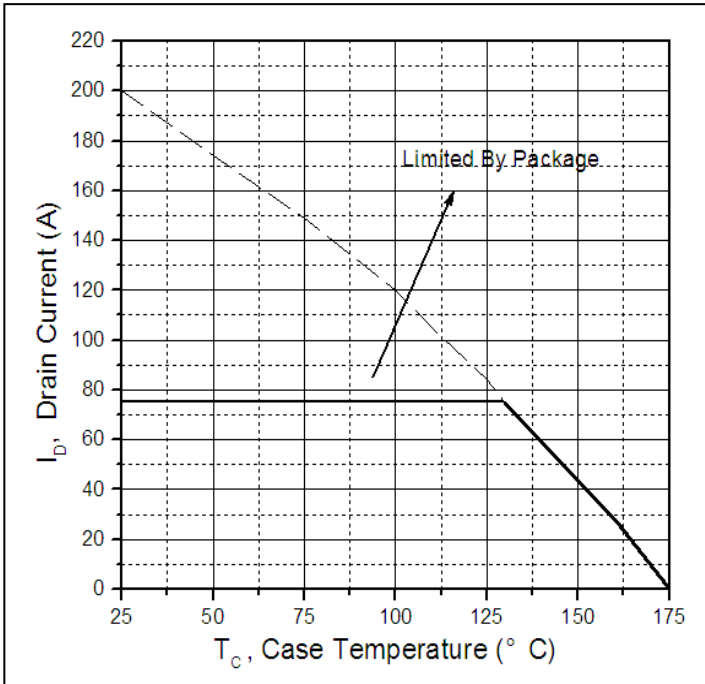


**Figure 3. Drain-to-Source Breakdown Voltage vs Case Temperature**

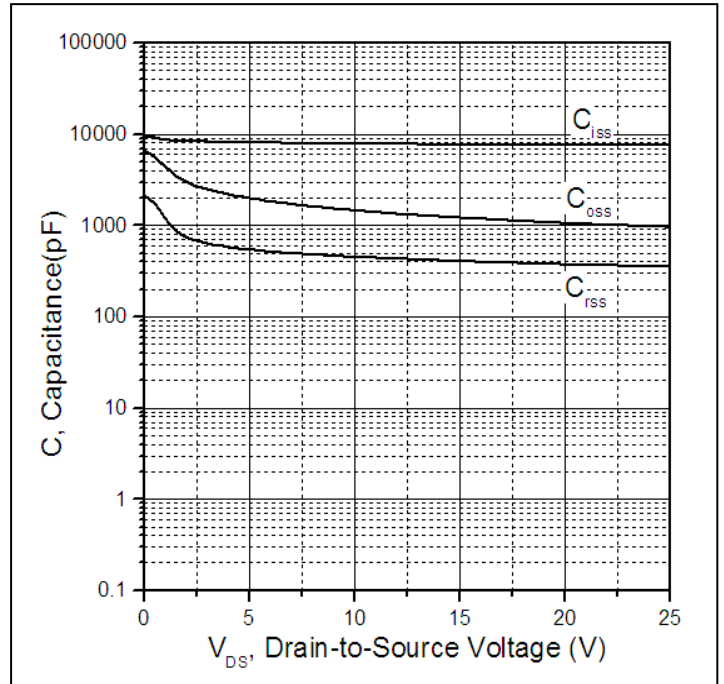


**Figure 4. Normalized On-Resistance Vs. Case Temperature**

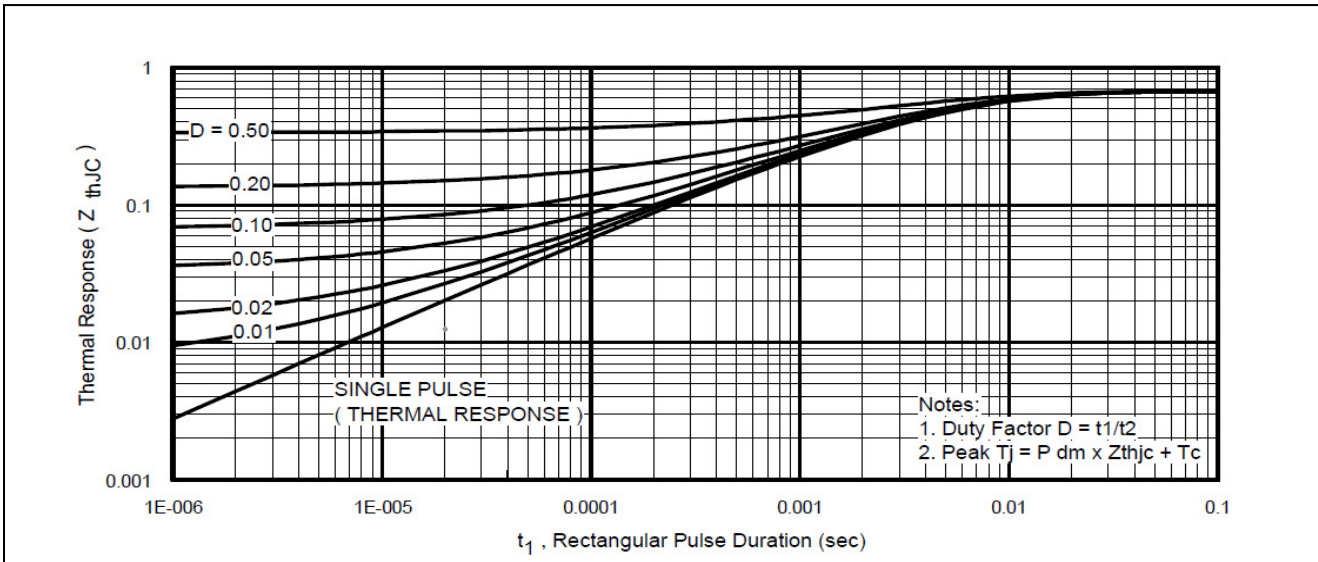
**Typical Electrical and Thermal Characteristics**



**Figure 5. Maximum Drain Current vs Case Temperature**



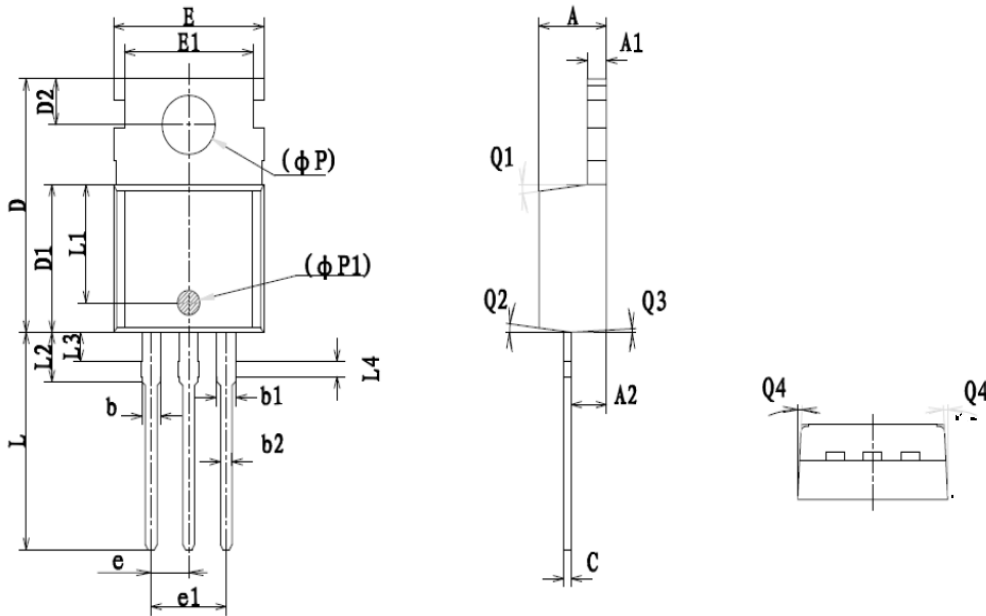
**Figure 6. Typical Capacitance vs Drain-to-Source Voltage**



**Figure 7. Maximum Effective Transient Thermal Impedance, Junction-to-Case**

**Mechanical Data**

TO-220 PACKAGE OUTLINE DIMENSIONS



Symbol	Dimension In Millimeters			Dimension In Inches		
	Min	Nom	Max	Min	Nom	Max
A	4.400	4.550	4.700	0.173	0.179	0.185
A1	1.270	1.300	1.330	0.050	0.051	0.052
A2	2.240	2.340	2.440	0.088	0.092	0.096
b	-	1.270	-	-	0	-
b1	1.270	1.370	1.470	0.050	0.054	0.058
b2	0.750	0.800	0.850	0.030	0.031	0.033
C	0.480	0.500	0.520	0.019	0.020	0.021
D	15.100	15.400	15.700	0.594	0.606	0.618
D1	8.800	8.900	9.000	0.346	0.350	0.354
D2	2.730	2.800	2.870	0.107	0.110	0.113
E	9.900	10.000	10.100	0.390	0.394	0.398
E1	-	8.700	-	-	0.343	-
φP	3.570	3.600	3.630	0.141	0.142	0.143
φP1	1.400	1.500	1.600	0.055	0.059	0.063
e	2.54BSC			0.1BSC		
e1	5.08BSC			0.2BSC		
L	13.150	13.360	13.570	0.518	0.526	0.534
L1	7.35REF			0.29REF		
L2	2.900	3.000	3.100	0.114	0.118	0.122
L3	1.650	1.750	1.850	0.065	0.069	0.073
L4	0.900	1.000	1.100	0.035	0.039	0.043
Q1	5°	7°	9°	5°	7°	9°
Q2	5°	7°	9°	5°	7°	9°
Q3	5°	7°	9°	5°	7°	9°
Q4	1°	3°	5°	1°	3°	5°

## Ordering and Marking Information

<b>Device Marking: SSFT4003</b>  Package (Available) TO-220  Operating Temperature Range C : -55 to 175 °C
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## Devices per Unit

Package Type	Units/ Tube	Tubes/ Inner Box	Units/ Inner Box	Inner Boxes/ Carton Box	Units/ Carton Box
TO-220	50	20	1000	10	10000

## Reliability Test Program

Test Item	Conditions	Duration	Sample Size
High Temperature Reverse Bias( $HT_{RB}$ )	$T_j=125^{\circ}\text{C}$ to $175^{\circ}\text{C}$ @ 80% of Max $V_{DSS}/V_{CES}/V_R$	168 hours 500 hours 1000 hours	3 lots x 77 devices
High Temperature Gate Bias( $HT_{GB}$ )	$T_j=150^{\circ}\text{C}$ or $175^{\circ}\text{C}$ @ 100% of Max $V_{GSS}$	168 hours 500 hours 1000 hours	3 lots x 77 devices