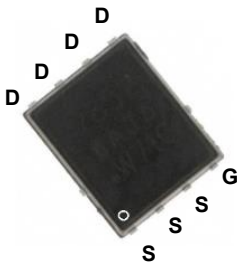
GOOD-ARK
SEMICONDUCTOR

# SSFP10N105

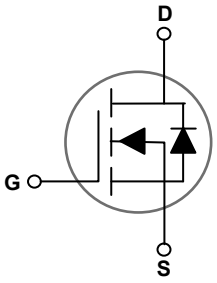
**100V N-Channel MOSFET**

## Main Product Characteristics

| | |
|---|---|
| $V_{(BR)DSS}$ | 100V |
| $R_{DS(ON)(Typ.)}$ | 5.6mΩ @$V_{GS}$=10V |
| $I_D$ | 105A |




PPAK5x6




Schematic Diagram

## Features and Benefits

- Advanced MOSFET process technology
- Ideal for high efficiency switched mode power supplies
- Low on-resistance with low gate charge
- Fast switching and reverse body recovery

RoHS Compliant

## Description

The SSFP10N105 utilizes the latest techniques to achieve high cell density and low on-resistance. These features make this device extremely efficient and reliable for use in high efficiency switch mode power supply and a wide variety of other applications.

## Absolute Maximum Ratings ($T_C$=25°C unless otherwise specified)

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| Drain-Source Voltage | $V_{DS}$ | 100 | V |
| Gate-Source Voltage | $V_{GS}$ | ±20 | V |
| Drain Current-Continuous | $I_D$ | 105 | A |
| Drain Current-Continuous($T_C$=100°C) | $I_D$ (100°C) | 74 | A |
| Pulsed Drain Current | $I_{DM}$ | 400 | A |
| Maximum Power Dissipation | $P_D$ | 135 | W |
| Derating Factor | | 1.1 | W/°C |
| Single Pulse Avalanche Energy[4] | $E_{AS}$ | 676 | mJ |
| Operating Junction and Storage Temperature Range | $T_J$,$T_{STG}$ | -55 To +150 | °C |

## Thermal Characteristics

| | | | |
|---|---|---|---|
| Thermal Resistance, Junction-to-Case[1] | $R_{\theta JC}$ | 0.93 | °C/W |

## Electrical Characteristics ($T_C$=25°C unless otherwise specified)

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Off Characteristics** | | | | | | |
| Drain-Source Breakdown Voltage | $BV_{DSS}$ | $V_{GS}$=0V, $I_D$=250μA | 100 | - | - | V |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{DS}$=100V, $V_{GS}$=0V | - | - | 1 | μA |
| Gate-Body Leakage Current | $I_{GSS}$ | $V_{GS}$=±20V, $V_{DS}$=0V | - | - | ±100 | nA |
| **On Characteristics[2]** | | | | | | |
| Gate Threshold Voltage | $V_{GS(th)}$ | $V_{DS}$=$V_{GS}$, $I_D$=250μA | 2.5 | - | 4.5 | V |
| Drain-Source On-State Resistance | $R_{DS(ON)}$ | $V_{GS}$=10V, $I_D$=50A | - | 5.6 | 6.4 | mΩ |
| Forward Transconductance | $g_{FS}$ | $V_{DS}$=10V, $I_D$=50A | 40 | - | - | S |
| **Dynamic Characteristics[3]** | | | | | | |
| Input Capacitance | $C_{lss}$ | $V_{DS}$=50V, $V_{GS}$=0V, F=1.0MHz | - | 4300 | - | PF |
| Output Capacitance | $C_{oss}$ | | - | 790 | - | |
| Reverse Transfer Capacitance | $C_{rss}$ | | - | 47 | - | |
| **Switching Characteristics[3]** | | | | | | |
| Turn-on Delay Time | $t_{d(on)}$ | $V_{DD}$=50V, $I_D$=50A, $V_{GS}$=10V, $R_G$=4.7Ω | - | 13 | - | nS |
| Turn-on Rise Time | $t_r$ | | - | 58 | - | |
| Turn-Off Delay Time | $t_{d(off)}$ | | - | 39 | - | |
| Turn-Off Fall Time | $t_f$ | | - | 8 | - | |
| Total Gate Charge | $Q_g$ | $V_{DS}$=50V, $I_D$=50A, $V_{GS}$=10V | - | 60 | - | nC |
| Gate-Source Charge | $Q_{gs}$ | | - | 21 | - | |
| Gate-Drain Charge | $Q_{gd}$ | | - | 11 | - | |
| **Drain-Source Diode Characteristics** | | | | | | |
| Diode Forward Voltage[2] | $V_{SD}$ | $V_{GS}$=0V, $I_S$=50A | - | - | 1.2 | V |
| Diode Forward Current[1] | $I_S$ | | - | - | 105 | A |
| Reverse Recovery Time | $t_{rr}$ | $T_J$=25°C, $I_F$=$I_S$, di/dt=100A/μS[2] | - | 60 | - | nS |
| Reverse Recovery Charge | Qrr | | - | 140 | - | nC |

Notes:

1. Surface Mounted on FR4 Board, t ≤ 10 sec.
2. Pulse Test: Pulse Width ≤ 300μS, Duty Cycle ≤ 2%.
3. Essentially independent of operating temperature.
4. $E_{AS}$ Condition: $T_J$=25°C, $V_{DD}$=50V, $V_G$=10V, L=0.5mH, Rg=25Ω

## Typical Electrical and Thermal Characteristic Curves

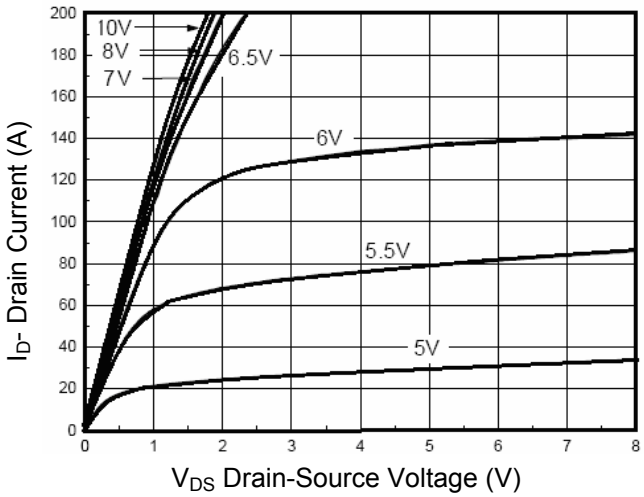



**Fig.1 Output Characteristics**

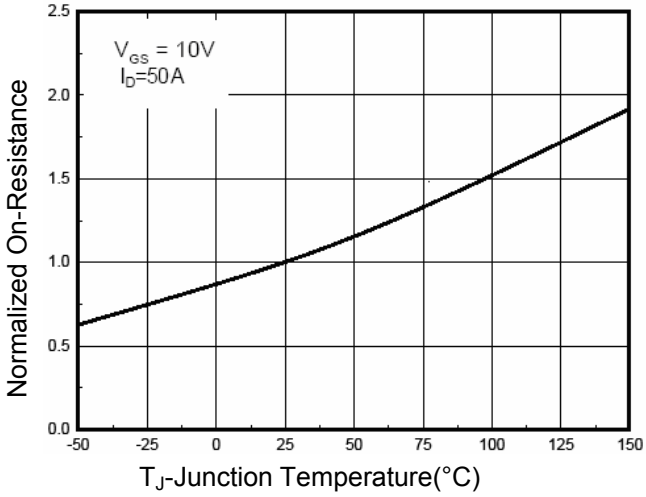



**Fig.2 $R_{DS(ON)}$-JunctionTemperature**

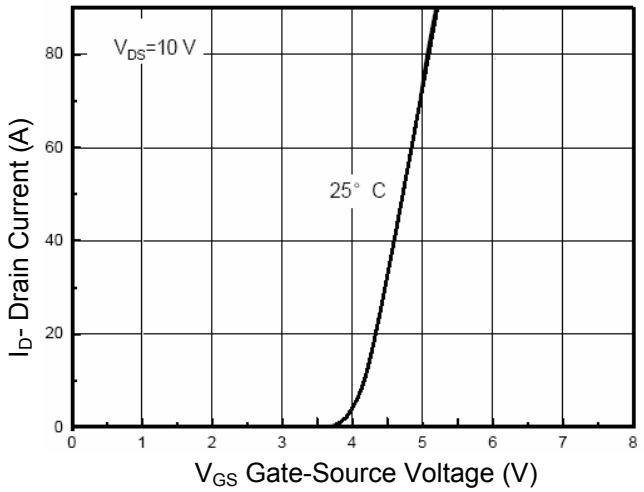



**Fig.3 Transfer Characteristics**

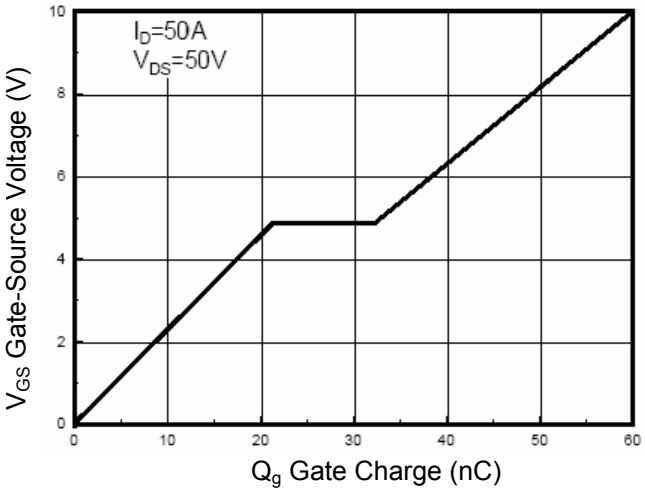



**Fig.4 Gate Charge**

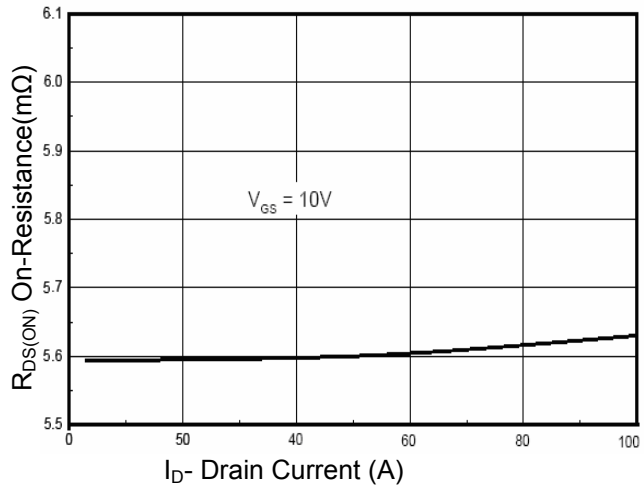



**Fig.5 $R_{DS(ON)}$- Drain Current**

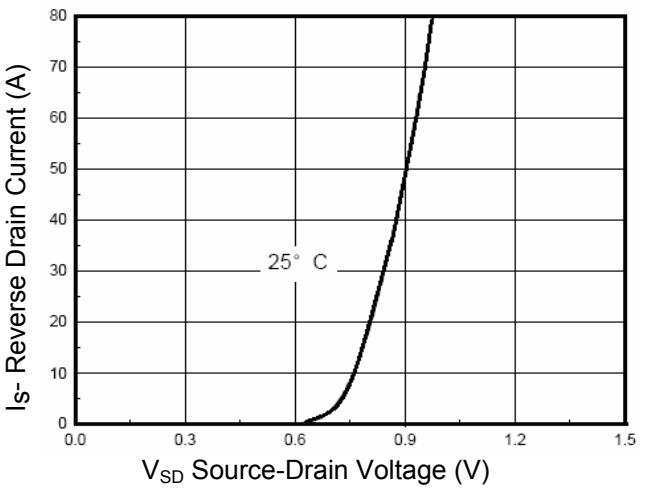



**Fig.6 Source- Drain Diode Forward**

## Typical Electrical and Thermal Characteristic Curves

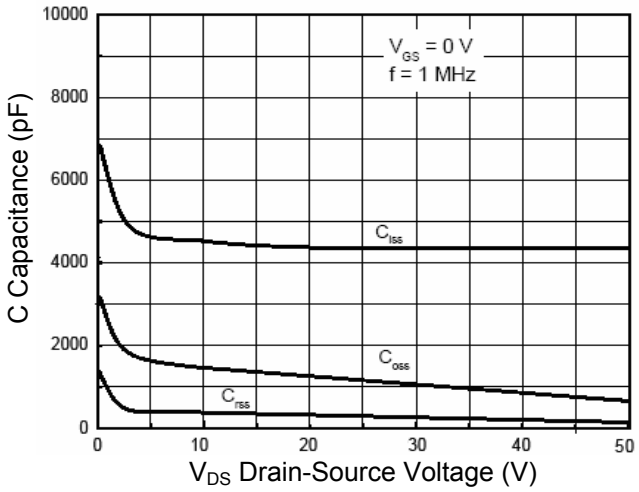



**Fig.7 Capacitance vs $V_{DS}$**

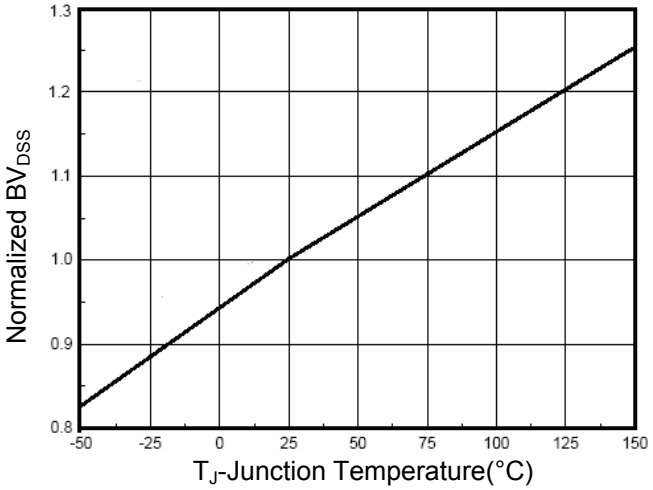



**Fig.8 $BV_{DSS}$ vs Junction Temperature**

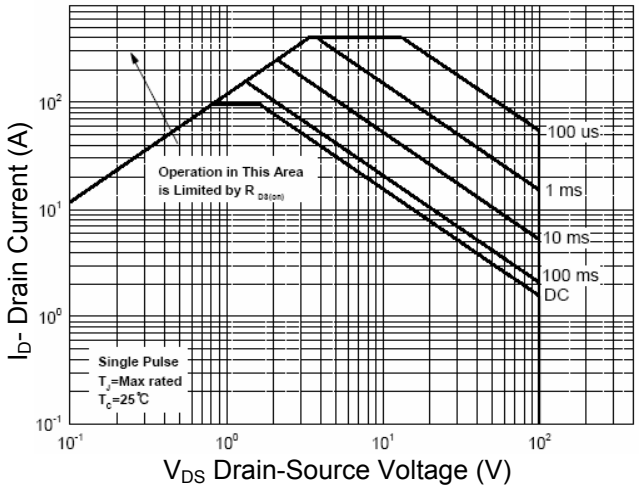



**Fig.9 Safe Operation Area**

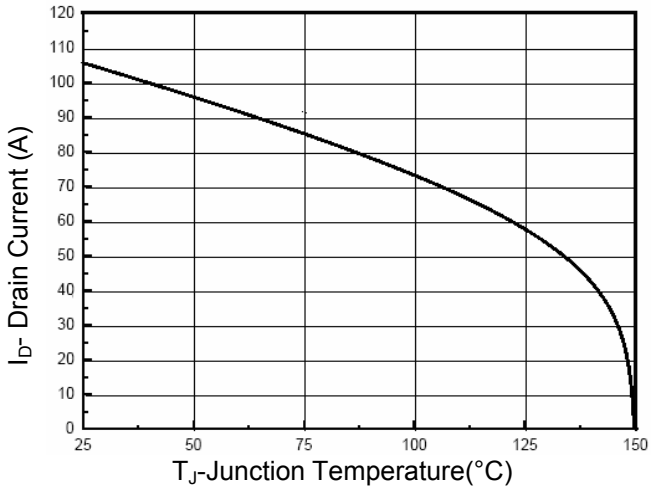



**Fig.10 Current De-rating**

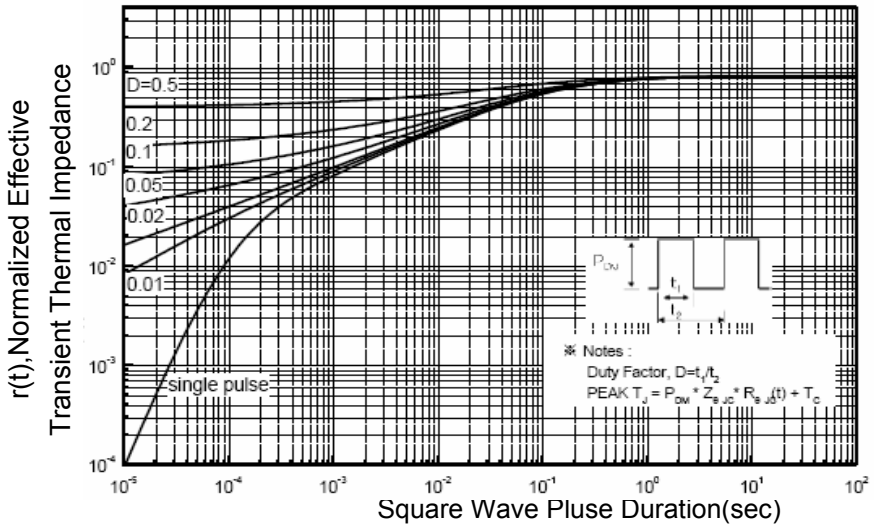



**Fig.11 Normalized Maximum Transient Thermal Impedance**

## Test Circuits

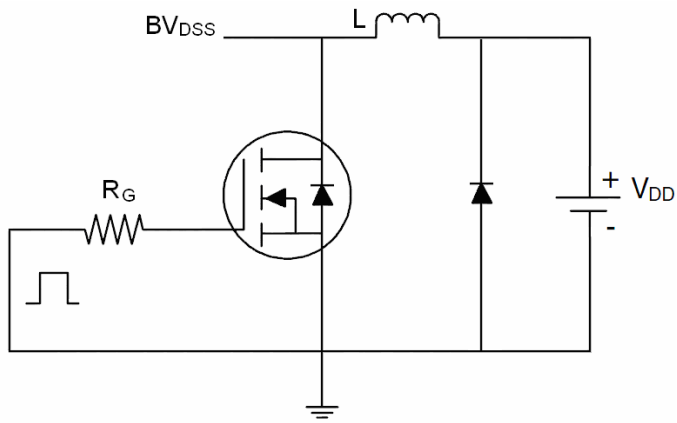



**Fig.12 $E_{AS}$ Test Circuit**

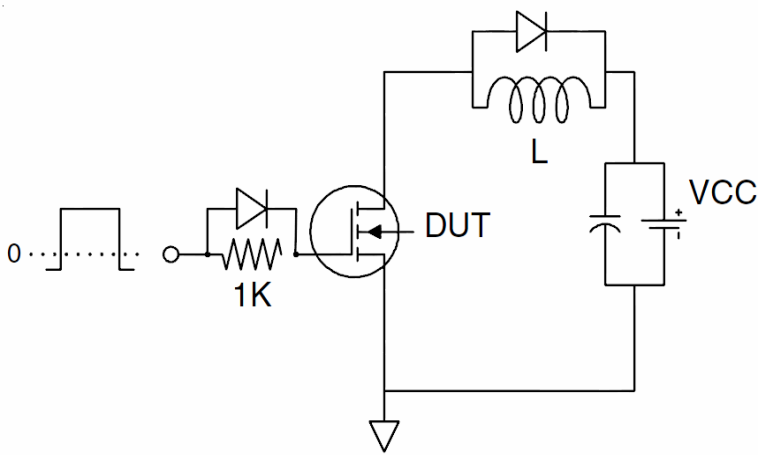



**Fig.13 Gate Charge Test Circuit**

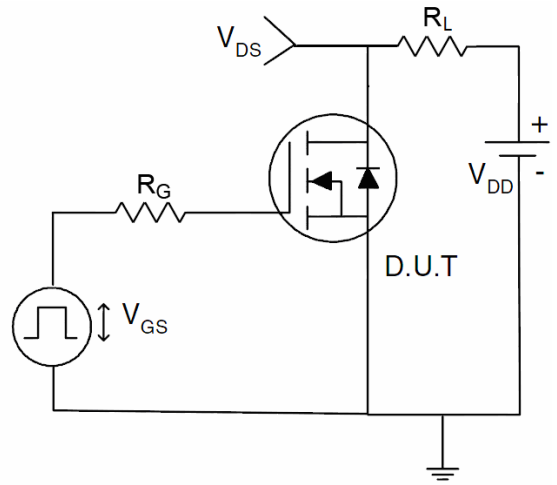
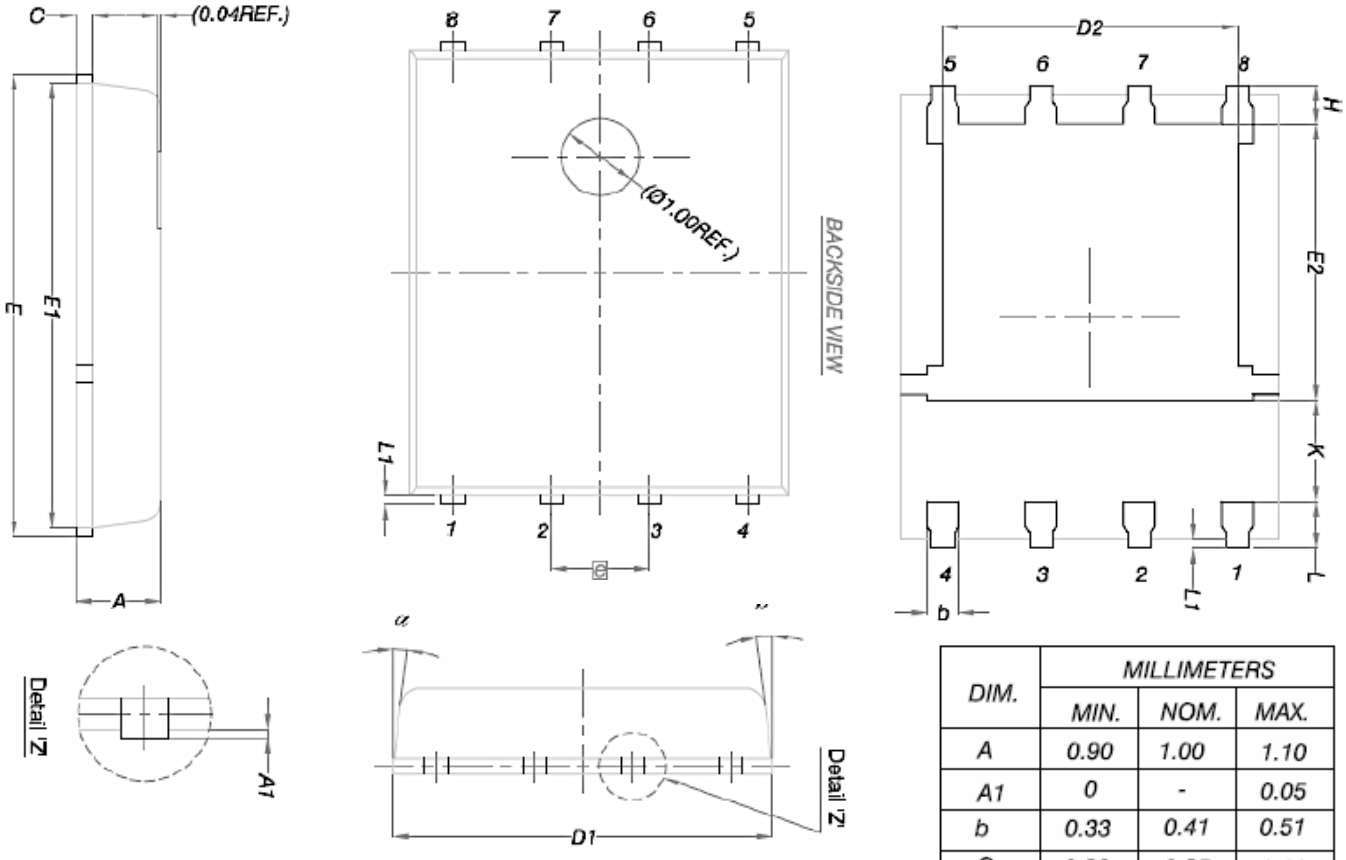



**Fig.14 Switch Time Test Circuit**

## Package Outline Dimensions PPAK5X6




| DIM. | MILLIMETERS | | |
|---|---|---|---|
| | MIN. | NOM. | MAX. |
| A | 0.90 | 1.00 | 1.10 |
| A1 | 0 | - | 0.05 |
| b | 0.33 | 0.41 | 0.51 |
| C | 0.20 | 0.25 | 0.30 |
| D1 | 4.80 | 4.90 | 5.00 |
| D2 | 3.61 | 3.81 | 3.96 |
| E | 5.90 | 6.00 | 6.10 |
| E1 | 5.70 | 5.75 | 5.80 |
| E2 | 3.38 | 3.58 | 3.78 |
| e | 1.27 BSC | | |
| H | 0.41 | 0.51 | 0.61 |
| K | 1.10 | - | - |
| L | 0.51 | 0.61 | 0.71 |
| L1 | 0.06 | 0.13 | 0.20 |
| α | 0° | - | 12° |

## Suggested Pad Layout

Unit: mm