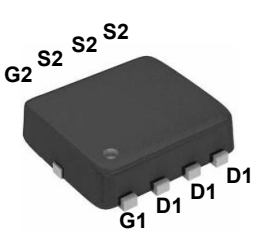
GOOD-ARK SEMICONDUCTOR

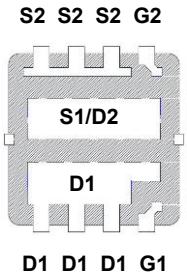
SSFN3810H

30V Dual N-Channel MOSFET

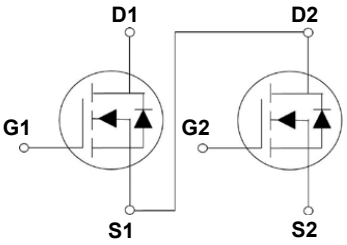
Main Product Characteristics

V_{DSS}	30V
$R_{DSON(max.)}$	10.5mΩ
I_D	19.5A





PPAK3X3



Schematic Diagram

Features and Benefits

- Advanced MOSFET process technology
- Ideal for high efficiency switched mode power supplies
- Low on-resistance with low gate charge
- Fast switching and reverse body recovery

Description

The SSFN3810H utilizes the latest techniques to achieve high cell density and low on-resistance. These features make this device extremely efficient and reliable for use in high efficiency switch mode power supply and a wide variety of other applications.

Absolute Maximum Ratings (T_C=25°C unless otherwise specified)

Parameter	Symbol	Rating	Unit
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	±20	V
Drain Current – Continuous (T_C=25°C)	I_D	19.5	A
Drain Current – Continuous (T_C=100°C)		12.3	A
Drain Current – Continuous (T_A=25°C)		10.8	A
Drain Current – Continuous (T_A=100°C)		6.8	A
Drain Current – Pulsed[1]	I_{DM}	78	A
Single Pulse Avalanche Energy[2]	E_{AS}	13	mJ
Single Pulse Avalanche Current[2]	I_{AS}	16	A
Power Dissipation (T_C=25°C)	P_D	27	W
Power Dissipation – Derate above 25°C		0.01	W/°C
Storage Temperature Range	T_{STG}	-55 to +150	°C
Operating Junction Temperature Range	T_J	-55 to +150	°C

Thermal Characteristics

Parameter	Symbol	Typ.	Max.	Unit
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	---	62	°C/W
Thermal Resistance Junction to Case	$R_{\theta JC}$	---	4.6	°C/W

Electrical Characteristics (T_J=25°C unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Static State Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_D=250uA	30	---	---	V
BV_{DSS} Temperature Coefficient	$\triangle BV_{DSS}/\triangle T_J$	Reference to 25°C, I_D=1mA	---	0.04	---	V/°C
Drain-Source Leakage Current	I_{DSS}	V_{DS}=30V , V_{GS}=0V, T_J=25°C	---	---	1	uA
		V_{DS}=24V, V_{GS}=0V, T_J=125°C	---	---	10	uA
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±20V, V_{DS}=0V	---	---	±100	nA
Static Drain-Source On-Resistance[3]	$R_{DS(ON)}$	V_{GS}=10V, I_D=10A	---	8.5	10.5	mΩ
		V_{GS}=4.5V, I_D=5A	---	11	14	mΩ
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS}=V_{DS}, I_D =250uA	1.2	1.6	2.5	V
$V_{GS(th)}$ Temperature Coefficient	$\triangle V_{GS(th)}$		---	-4	---	mV/°C
Forward Transconductance	gfs	V_{DS}=5V, I_D=5A	---	12	---	S
Dynamic Characteristics						
Total Gate Charge[3, 4]	Q_g	V_{DS}=15V, V_{GS}=10V , I_D=5A	---	15.6	31	nC
Gate-Source Charge[3, 4]			---	2.3	5	
Gate-Drain Charge[3, 4]	Q_{gd}		---	3	6	
Turn-On Delay Time[3, 4]	$T_{d(on)}$	V_{DD}=15V, V_{GS}=10V, R_G=6Ω, I_D=1A	---	3.8	7	nS
Rise Time[3, 4]	T_r		---	10	19	
Turn-Off Delay Time[3, 4]	$T_{d(off)}$		---	22	42	
Fall Time[3, 4]	T_f		---	6.6	13	
Input Capacitance	C_{iss}	V_{DS}=25V, V_{GS}=0V, F=1MHz	---	620	900	pF
Output Capacitance	C_{oss}		---	85	125	
Reverse Transfer Capacitance	C_{rss}		---	60	90	
Gate Resistance	R_g	V_{GS}=0V, V_{DS}=0V, F=1MHz	---	2.8	5.6	Ω
Drain-Source Diode Characteristics						
Continuous Source Current	I_S	V_G=V_D=0V, Force Current	---	---	19.5	A
Pulsed Source Current[3]	I_{SM}		---	---	39	A
Diode Forward Voltage[3]	V_{SD}	V_{GS}=0V, I_S=1A, T_J=25°C	---	---	1	V

Note:
1. Repetitive Rating: Pulsed width limited by maximum junction temperature.
2. V_{DD}=25V, V_{GS}=10V, L=0.1mH, Q1: I_{AS}=16A, Q2: I_{AS}=42A, R_G=25Ω, Starting T_J=25°C.
3. The data tested by pulsed, pulse width ≦ 300 uS, duty cycle ≦ 2%.
4. Essentially independent of operating temperature.

Typical Electrical and Thermal Characteristic Curves

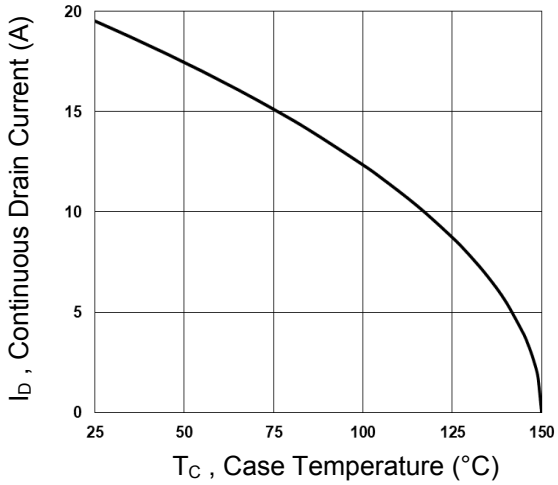


Fig.1 Continuous Drain Current vs. T_C

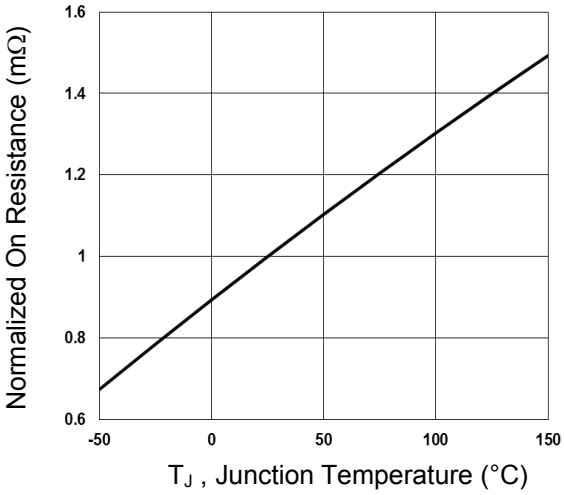


Fig.2 Normalized $R_{DS(ON)}$ vs. T_J

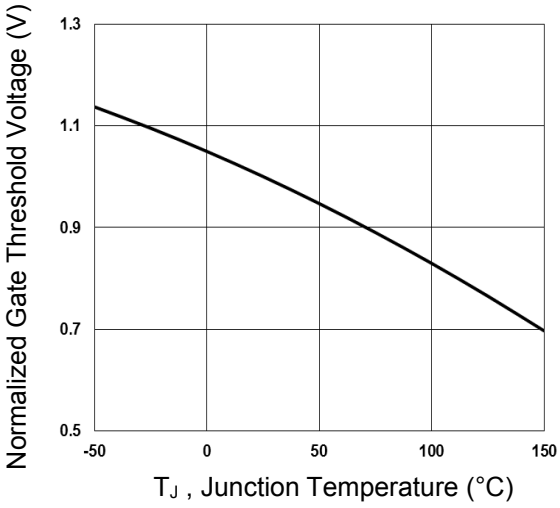


Fig.3 Normalized V_{th} vs. T_J

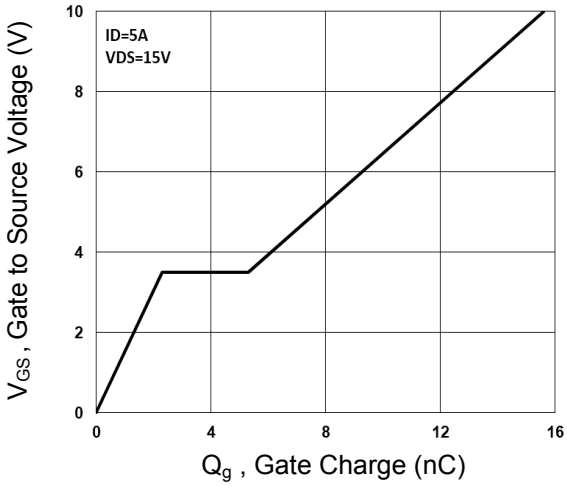


Fig.4 Gate Charge Waveform

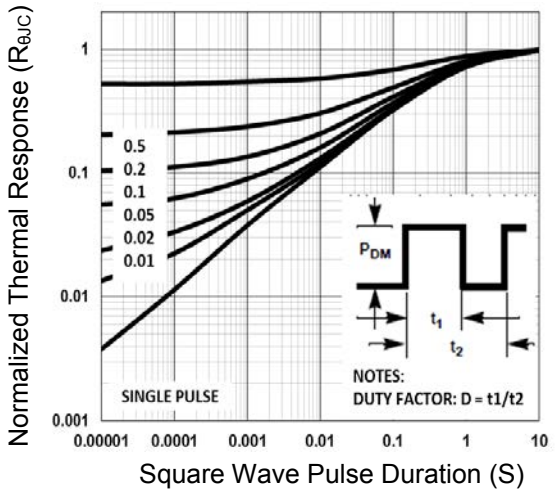


Fig.5 Normalized Transient Impedance

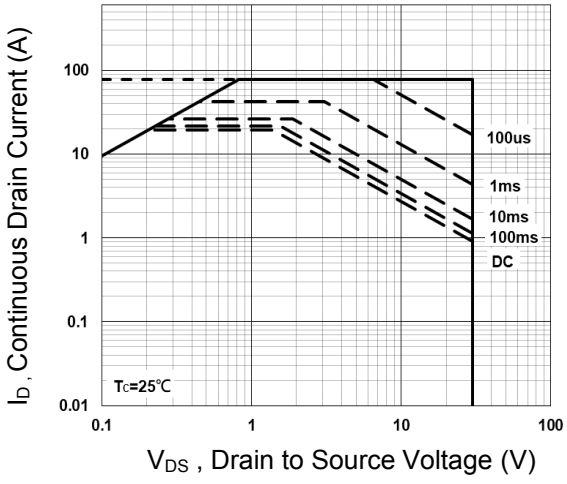


Fig.6 Maximum Safe Operation Area

Typical Electrical and Thermal Characteristic Curves

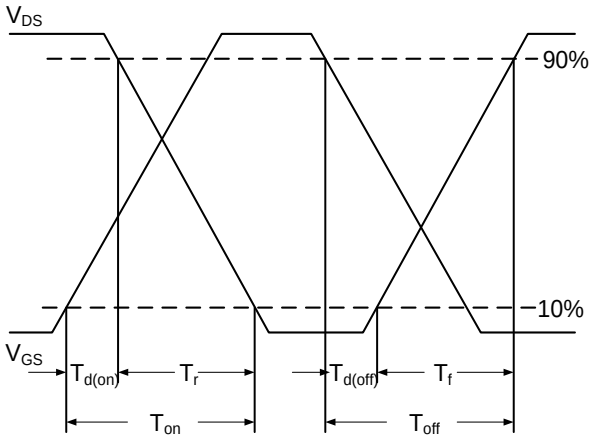


Fig.7 Switching Time Waveform

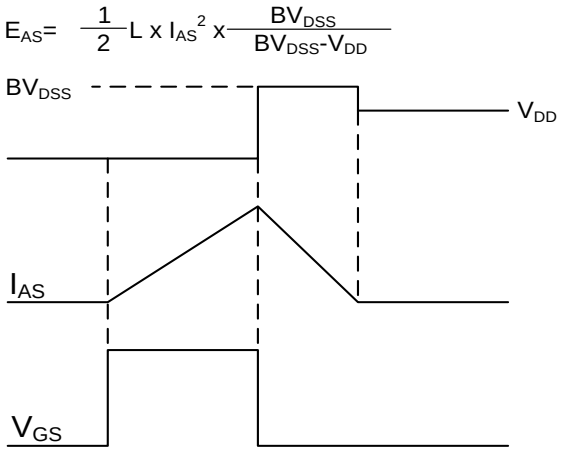
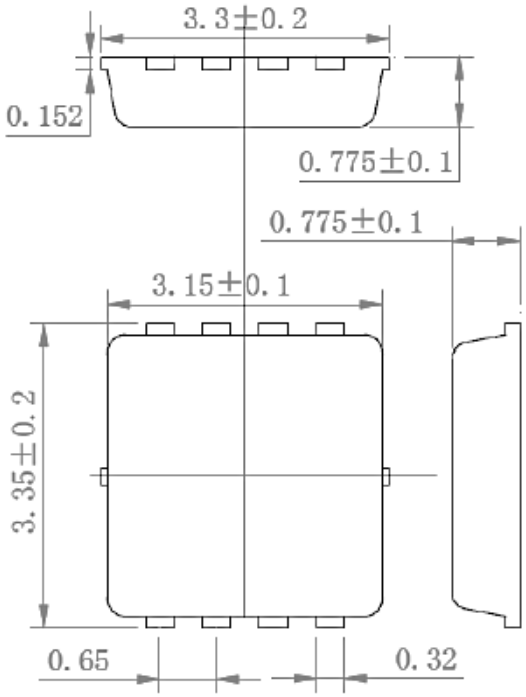
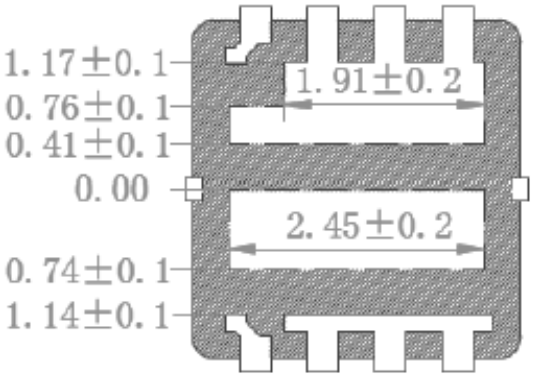


Fig.8 E_{AS} Waveform

Package Outline Dimensions



PPAK3X3 Asymmetric Dual Pin



Suggested Pad Layout