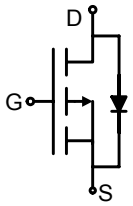
GOOD-ARK SEMICONDUCTOR

SSFD6035

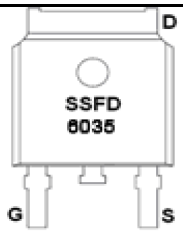
60V P-Channel MOSFET

DESCRIPTION

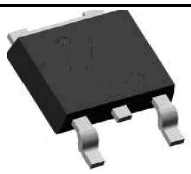
The SSFD6035 uses advanced trench technology to provide excellent $R_{DS(ON)}$ and low gate charge .This device is suitable for use as a load switch or in PWM applications.



Schematic Diagram



Marking and Pin Assignment



TO-252/DPAK (Top View)

FEATURES

- V_{DS} =- 60V,I_D =-26A
  $R_{DS(ON)}$ < 40mΩ @ V_{GS}=-10V
  $R_{DS(ON)}$ < 55mΩ @ V_{GS}=-4.5V
- High Power and Current Handling Capability
- Lead Free
- Surface Mount Package

APPLICATIONS

- PWM Applications
- Load Switch
- Power Management

PACKAGE MARKING

Device Marking	Device	Device Package
SSFD6035	SSFD6035	TO-252(DPAK)

ABSOLUTE MAXIMUM RATINGS (T_A=25°C unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	-60	V
Gate-Source Voltage	V_{GS}	±20	V
Drain Current-Continuous@ Current-Pulsed (Note 1)	I_D(25°C)	-26	A
	I_D(70°C)	-20	A
	I_{DM}	-60	A
Maximum Power Dissipation	P_D	60	W
Operating Junction and Storage Temperature Range	T_J,T_{STG}	-55 To 175	°C

THERMAL CHARACTERISTICS

Thermal Resistance, Junction-to-Ambient (Note 2)	$R_{\theta JA}$	25	°C/W

ELECTRICAL CHARACTERISTICS (T_A=25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V I_D=-250μA	-60			V

Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-48V,V_{GS}=0V			-1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±20V,V_{DS}=0V			±100	nA
ON CHARACTERISTICS (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=-250μA	-1	-1.8	-2.5	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=-10V, I_D=-20A		31	40	mΩ
		V_{GS}=-4.5V, I_D=-20A		42	55	mΩ
Forward Transconductance	g_{FS}	V_{DS}=-5V,I_D=-20A	5			S
DYNAMIC CHARACTERISTICS (Note 4)						
Input Capacitance	C_{lss}	V_{DS}=-30V,V_{GS}=0V, F=1.0MHz		3060		PF
Output Capacitance	C_{oss}			300		PF
Reverse Transfer Capacitance	C_{rss}			205		PF
SWITCHING CHARACTERISTICS (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	V_{DS}=-30V,V_{GS}=-10V,R_{GEN}=3Ω I_D=1A		14		nS
Turn-on Rise Time	t_r			20		nS
Turn-Off Delay Time	$t_{d(off)}$			40		nS
Turn-Off Fall Time	t_f			19		nS
Total Gate Charge	Q_g	V_{DS}=-30V,I_D=-20A,V_{GS}=-10V		48		nC
Gate-Source Charge	Q_{gs}			11		nC
Gate-Drain Charge	Q_{gd}			10		nC
Body Diode Reverse Recovery Time	T_{rr}	I_F=-20A, dI/dt=100A/μs		40		nS
Body Diode Reverse Recovery Charge	Q_{rr}			56		nC
DRAIN-SOURCE DIODE CHARACTERISTICS						
Diode Forward Voltage (Note 3)	V_{SD}	V_{GS}=0V,I_S=-1A		-0.72	-1	V

NOTES:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on 1in^2 FR4 Board, t ≤ 10 sec.
3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production testing.

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

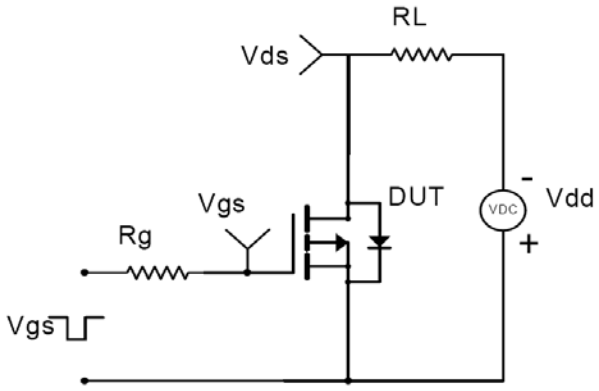


Figure 1. Switching Test Circuit

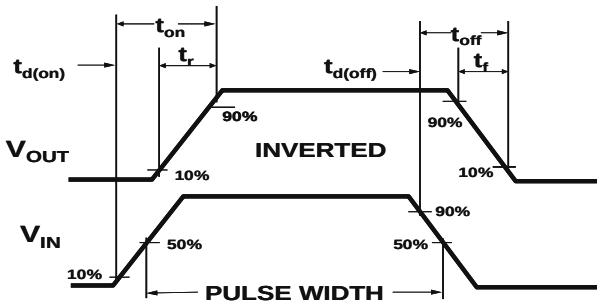


Figure 2. Switching Waveforms

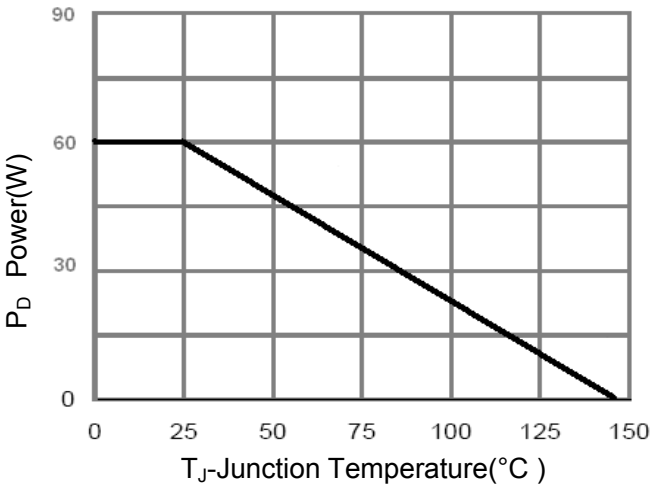


Figure 3. Power Dissipation

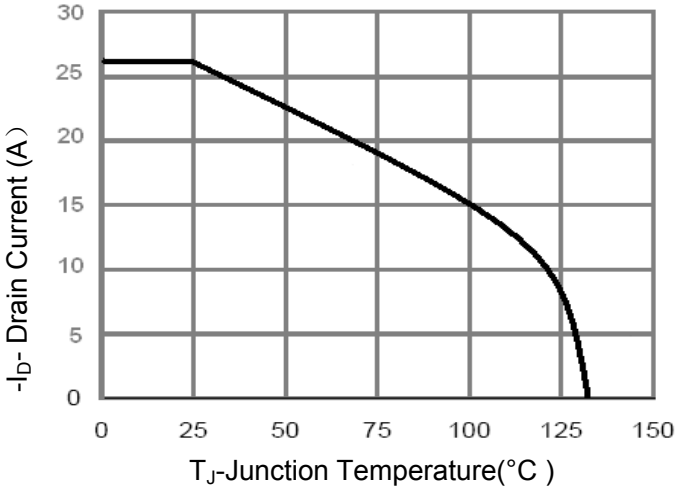


Figure 4. Drain Current

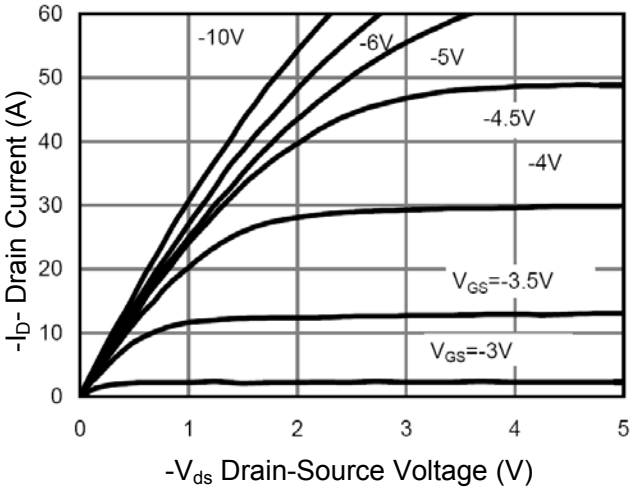


Figure 5. Output Characteristics

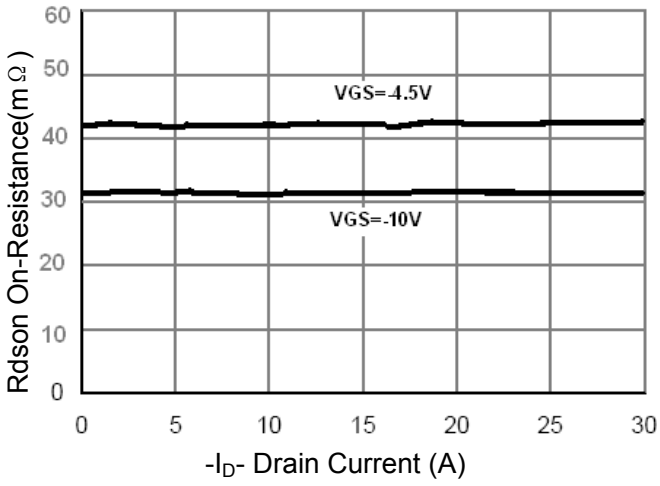


Figure 6. Drain-Source On-Resistance

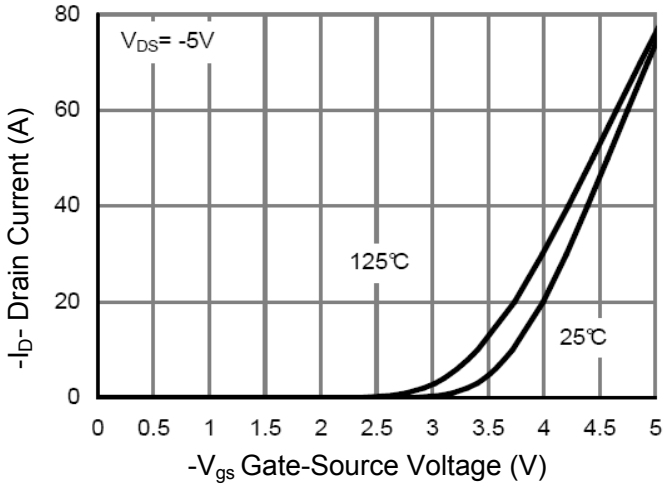


Figure 7. Transfer Characteristics

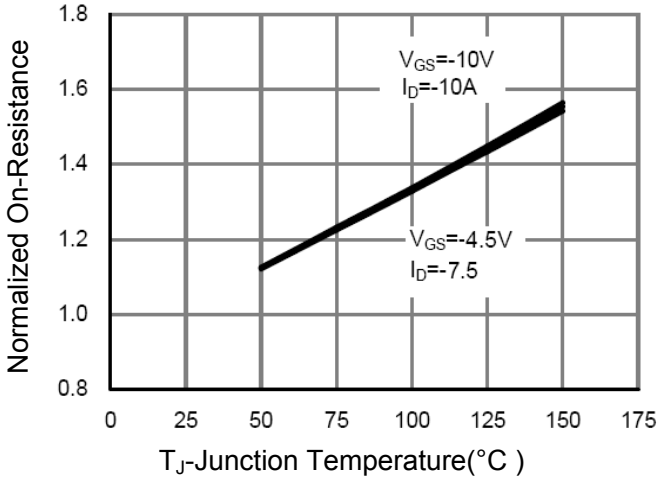


Figure 8. Drain-Source On-Resistance

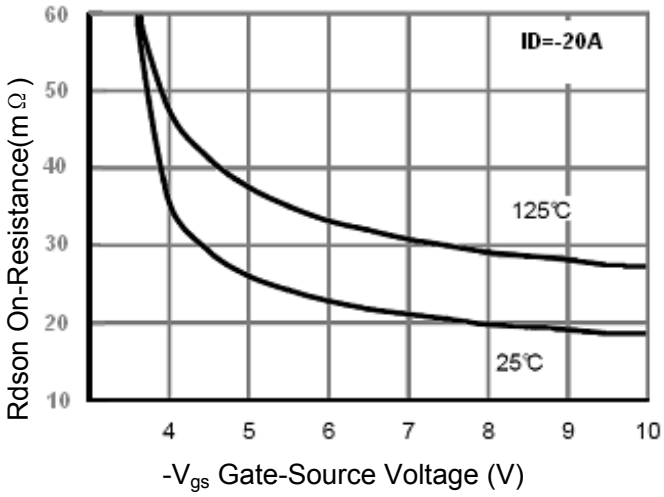


Figure 9. $R_{ds(on)}$ vs V_{gs}

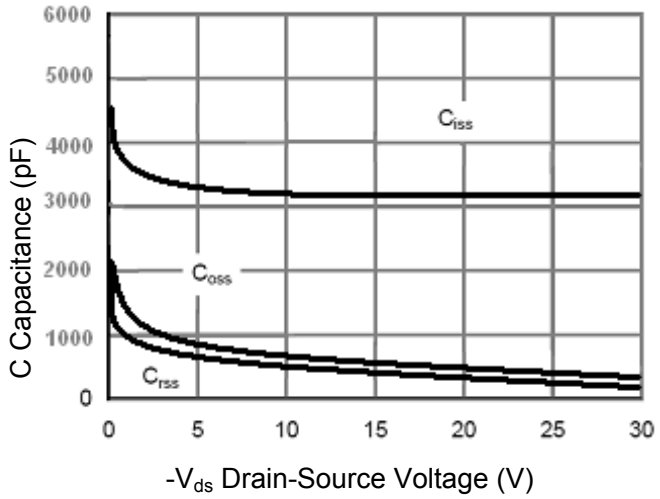


Figure 10. Capacitance vs V_{ds}

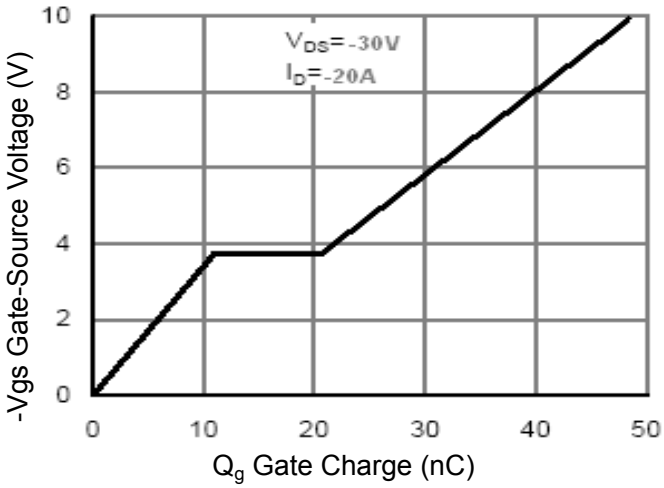


Figure 11. Gate Charge

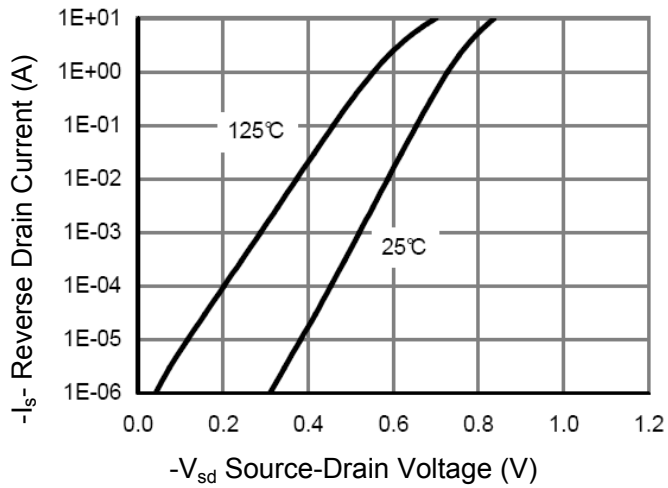


Figure 12. Source- Drain Diode Forward

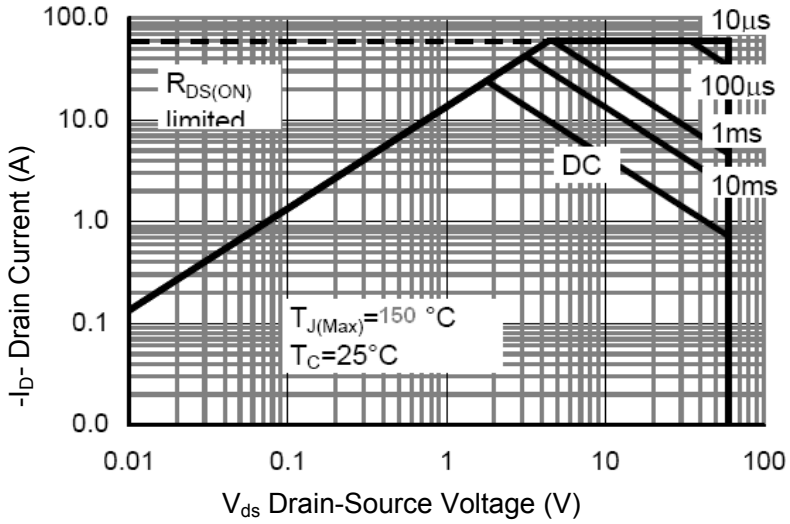


Figure 13. Safe Operation Area

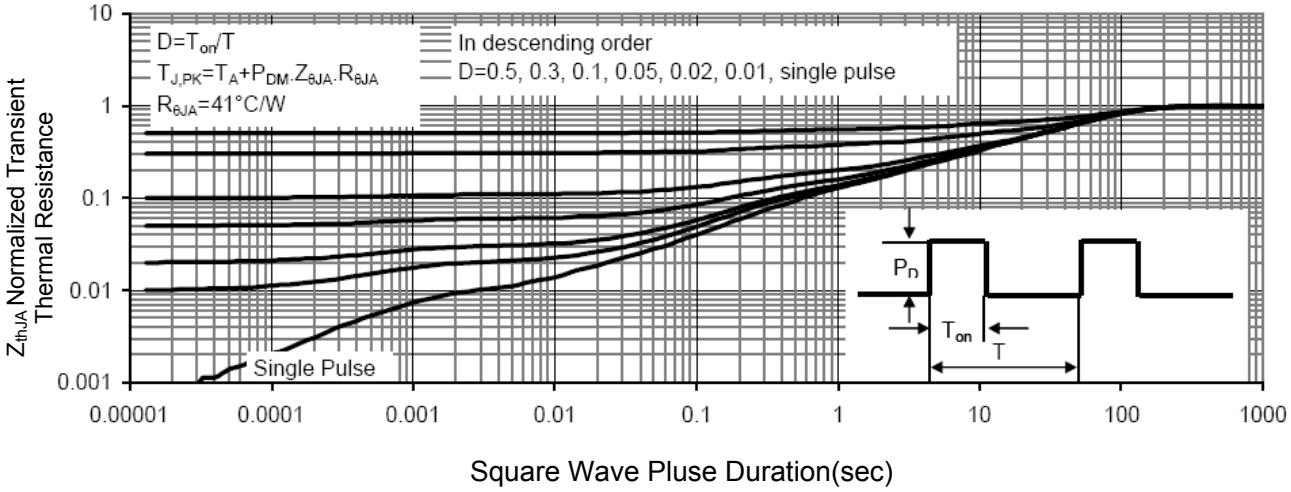
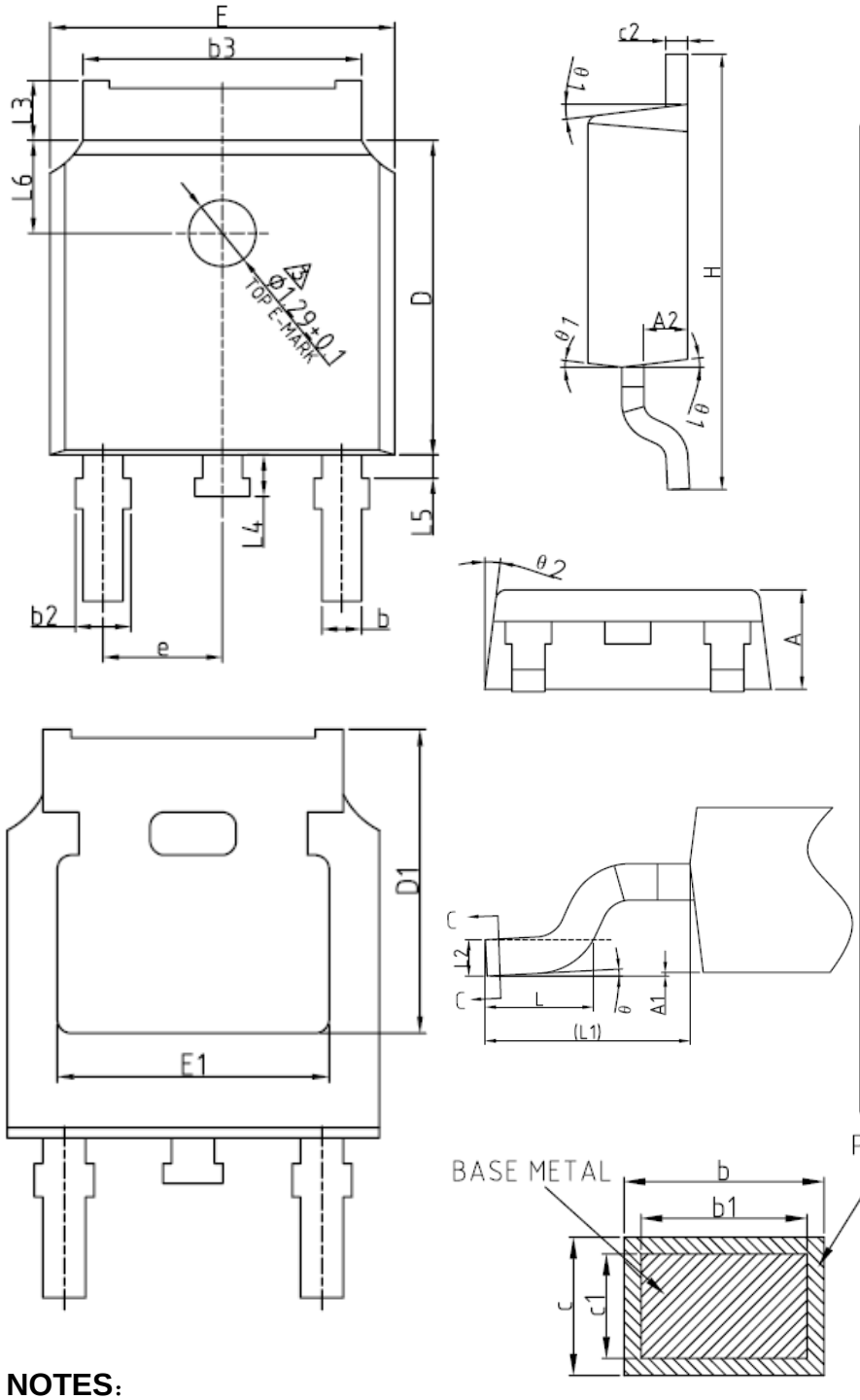


Figure 14. Normalized Maximum Transient Thermal Impedance

DPAK PACKAGE OUTLIE DIMENSIONS



Dimensions in Millimeters

SYMBOL	MIN	NOM	MAX
A	2.20	2.30	2.38
A1	0	–	0.10
A2	0.90	1.01	1.10
b	0.72	–	0.85
b1	0.71	0.76	0.81
b2	0.72	–	0.90
b3	5.13	5.33	5.46
c	0.47	–	0.60
c1	0.46	0.51	0.56
c2	0.47	–	0.60
D	6.00	6.10	6.20
D1	5.25	–	–
E	6.50	6.60	6.70
E1	4.70	–	–
e	2.186	2.286	2.386
H	9.80	10.10	10.40
L	1.40	1.50	1.70
L1	2.90REF		
L2	0.51BSC		
L3	0.90	–	1.25
L4	0.60	0.80	1.00
L5	0.15	–	0.75
L6	1.80REF		
θ	0°	–	8°
θ1	5°	7°	9°
θ2	5°	7°	9°

NOTES:

1. Dimensions are inclusive of plating.
2. Package body sizes exclude mold flash and gate burrs. Mold flash at the non-lead sides should be less than 6 mils.
3. Dimension L is measured in gauge plane.
4. Controlling dimension is millimeter, converted inch dimensions are not necessarily exact.