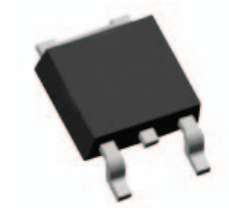
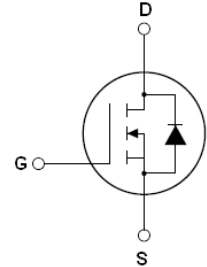


### Main Product Characteristics

$V_{DS}$	40V
$R_{DS(ON)}$	13mΩ (Max) @ $V_{GS}=10\text{ V}$
$I_D$	60A



TO-252(DPAK)



Schematic Diagram

### Features and Benefits

- Advanced MOSFET process technology
- Low on-resistance
- Fast switching and reverse body recovery



### Description

The SSFD4060 utilizes the latest techniques to achieve high cell density and low on-resistance. These features make this device extremely efficient and reliable for use in high efficiency switch mode power supply and a wide variety of other applications.

### Absolute Maximum Ratings ( $T_C=25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Value	Unit
Drain-Source Voltage	$V_{DS}$	40	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Drain Current-Continuous	$I_D$	60	A
Drain Current-Continuous ( $T_C=100^\circ\text{C}$ )	$I_{D(100^\circ\text{C})}$	42	A
Pulsed Drain Current	$I_{DM}$	200	A
Maximum Power Dissipation	$P_D$	65	W
Power Dissipation-Derating Factor		0.43	W/ $^\circ\text{C}$
Single Pulse Avalanche Energy <sup>4</sup>	$E_{AS}$	400	mJ
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 to +175	$^\circ\text{C}$
Thermal Resistance, Junction-to-Case <sup>1</sup>	$R_{\theta JC}$	2.3	$^\circ\text{C}/\text{W}$

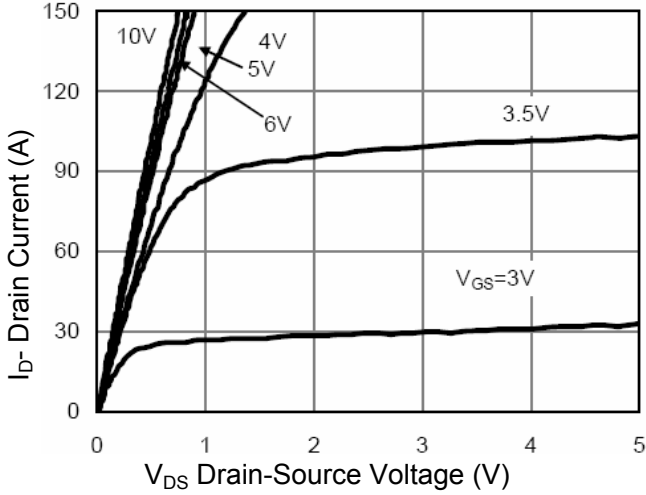
**Electrical Characteristics** ( $T_C=25^\circ\text{C}$  unless otherwise specified)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS}=0V, I_D=250\mu A$	40	45	-	V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=40V, V_{GS}=0V$	-	-	1	$\mu A$
Gate-Body Leakage Current	$I_{GSS}$	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	$\pm 100$	nA
<b>On Characteristics<sup>2</sup></b>						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1.2	1.6	2.5	V
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=20A$	-	7.3	13	m $\Omega$
Forward Transconductance	$g_{FS}$	$V_{DS}=10V, I_D=20A$	15	-	-	S
<b>Dynamic Characteristics<sup>3</sup></b>						
Input Capacitance	$C_{iss}$	$V_{DS}=20V, V_{GS}=0V,$ $F=1.0\text{MHz}$	-	1800	-	PF
Output Capacitance	$C_{oss}$		-	280	-	PF
Reverse Transfer Capacitance	$C_{rss}$		-	190	-	PF
<b>Switching Characteristics<sup>3</sup></b>						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=20V, I_D=2A, R_L=1\Omega$ $V_{GS}=10V, R_G=3\Omega$	-	6.4	-	nS
Turn-on Rise Time	$t_r$		-	17.2	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	29.6	-	nS
Turn-Off Fall Time	$t_f$		-	16.8	-	nS
Total Gate Charge	$Q_g$	$V_{DS}=20V, I_D=20A,$ $V_{GS}=10V$	-	29	-	nC
Gate-Source Charge	$Q_{gs}$		-	4.5	-	nC
Gate-Drain Charge	$Q_{gd}$		-	6.4	-	nC
<b>Drain-Source Diode Characteristics</b>						
Diode Forward Voltage <sup>2</sup>	$V_{SD}$	$V_{GS}=0V, I_S=10A$	-	-	1.2	V
Diode Forward Current <sup>1</sup>	$I_S$		-	-	60	A
Reverse Recovery Time	$t_{rr}$	$T_J = 25^\circ\text{C}, I_F = 20A$ $di/dt = 100A/\mu S^3$	-	29	-	nS
Reverse Recovery Charge	$Q_{rr}$		-	26	-	nC
Forward Turn-On Time	$t_{on}$	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

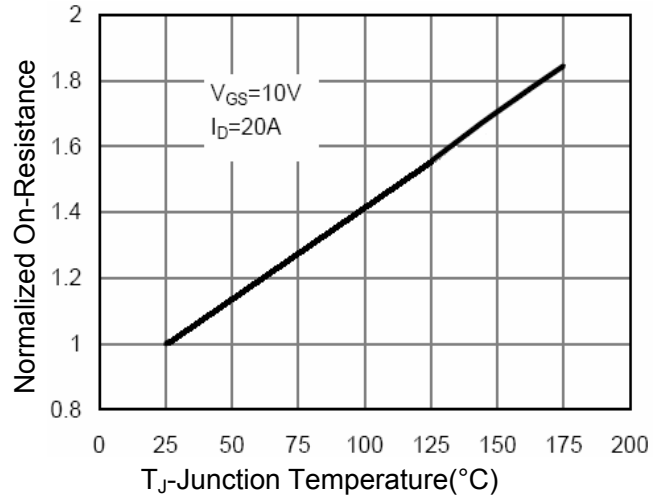
**Notes:**

1. Surface Mounted on FR4 Board,  $t \leq 10$  sec.
2. Pulse Test: Pulse Width  $\leq 300\mu S$ , Duty Cycle  $\leq 2\%$ .
3. Guaranteed by design, not subject to production
4.  $E_{AS}$  condition:  $T_J=25^\circ\text{C}, V_{DD}=20V, V_G=10V, L=1\text{mH}, R_G=25\Omega$

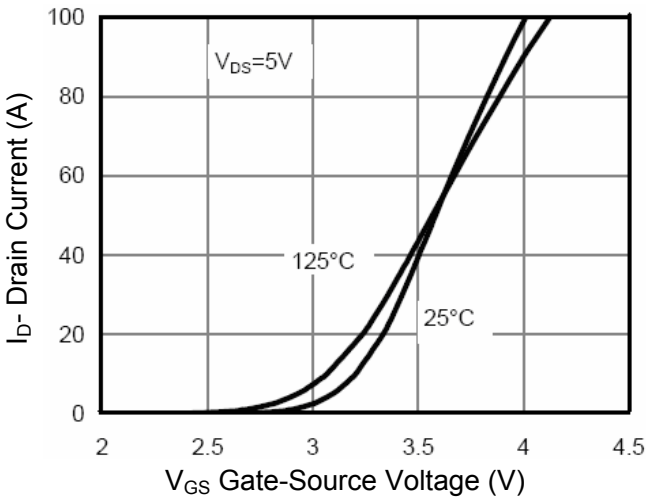
**Typical Electrical and Thermal Characteristic Curves**



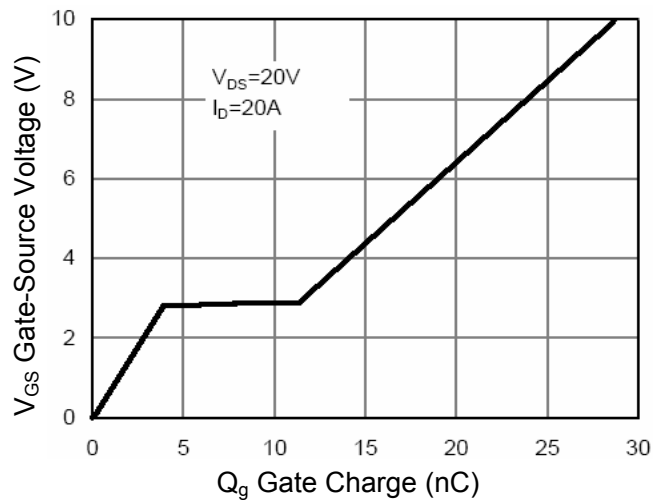
**Figure 1 Output Characteristics**



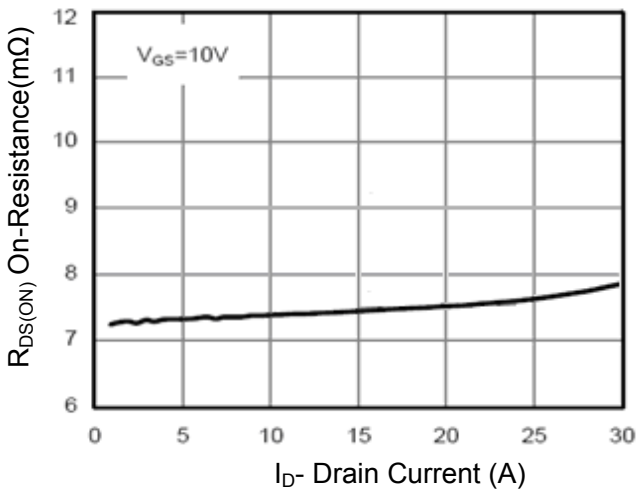
**Figure 2  $R_{DS(ON)}$ -Junction Temperature**



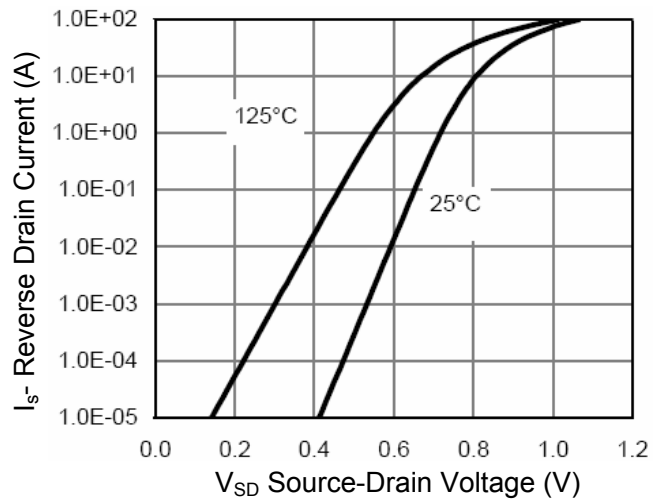
**Figure 3 Transfer Characteristics**



**Figure 4 Gate Charge**

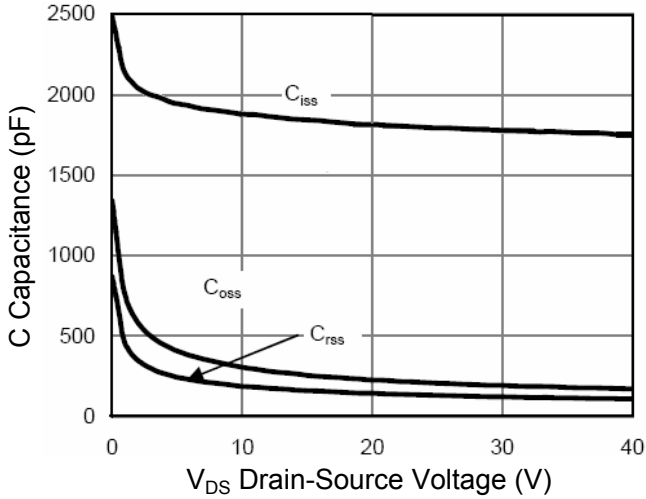


**Figure 5  $R_{DS(ON)}$ - Drain Current**

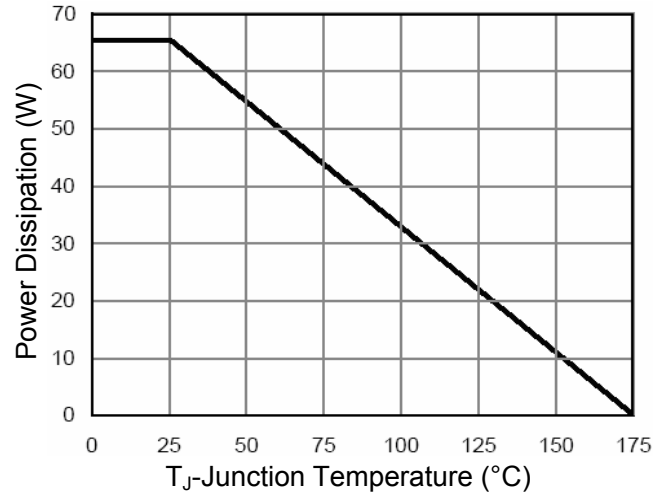


**Figure 6 Source- Drain Diode Forward**

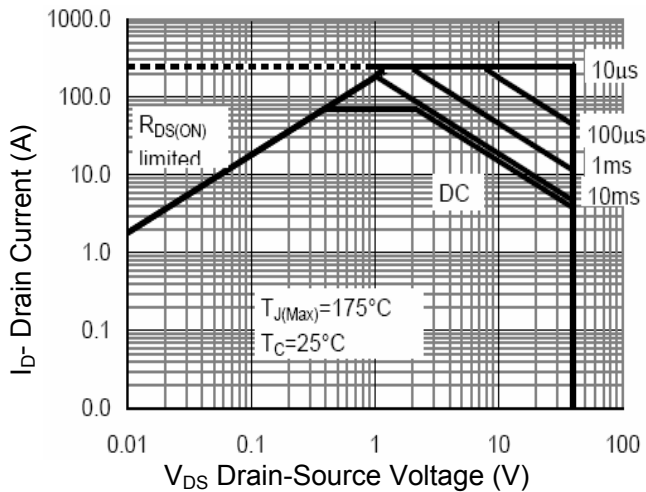
**Typical Electrical and Thermal Characteristic Curves**



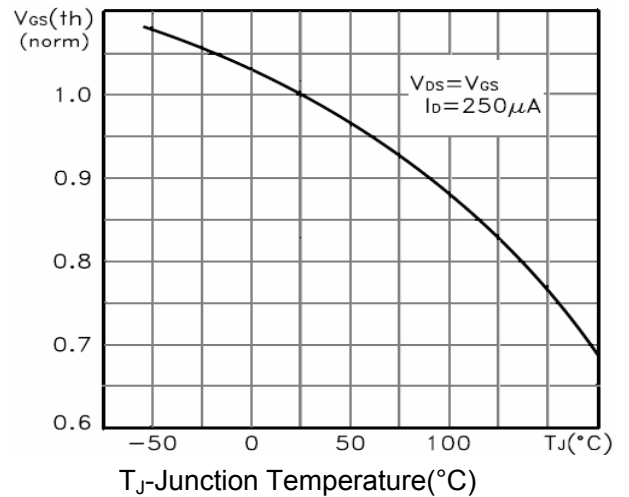
**Figure 7 Capacitance vs  $V_{DS}$**



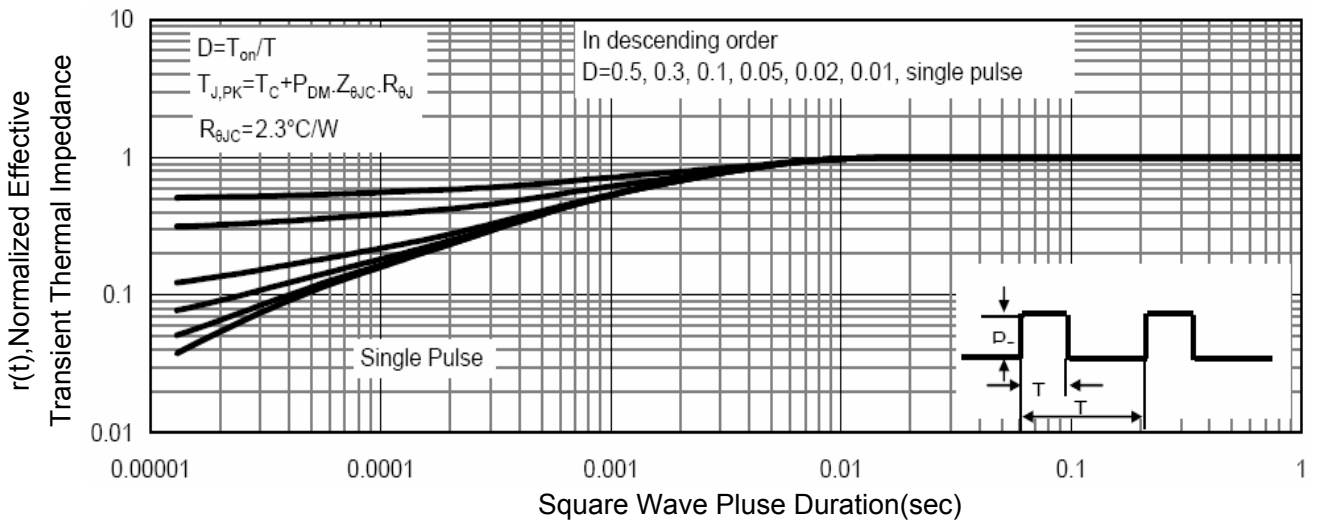
**Figure 8 Power De-rating**



**Figure 9 Safe Operation Area**

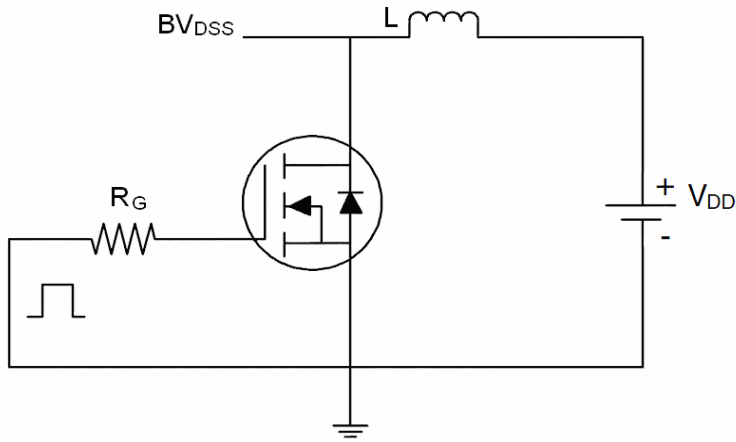


**Figure 10  $V_{GS(th)}$  vs Junction Temperature**

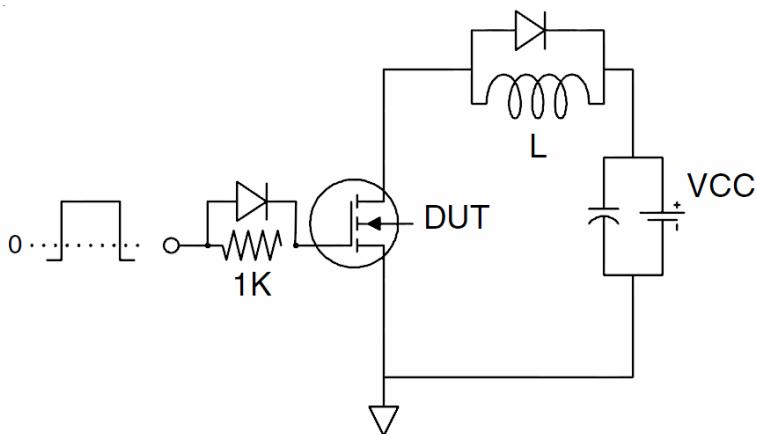


**Figure 11 Normalized Maximum Transient Thermal Impedance**

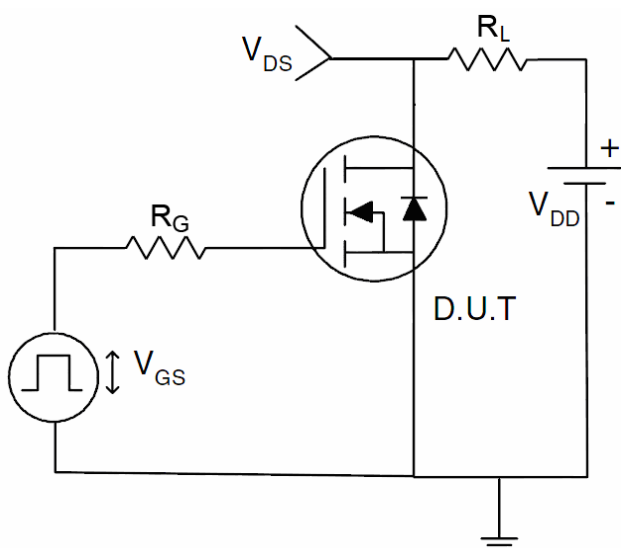
**Test Circuit**



**Figure 12  $E_{AS}$  Test Circuit**



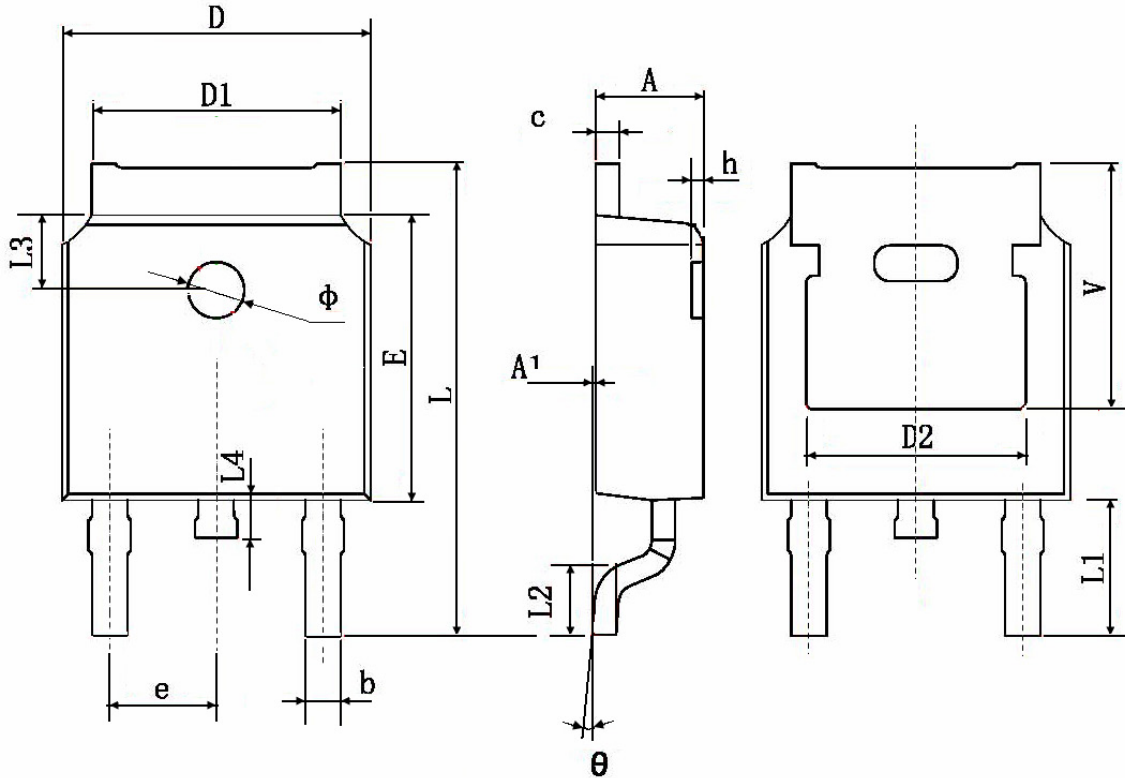
**Figure 13 Gate Charge Test Circuit**



**Figure 14 Switch Time Test Circuit**

**Package Outline Dimensions**

**TO-252(DPAK)**



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	2.200	2.400	0.087	0.094
A1	0.000	0.127	0.000	0.005
b	0.660	0.860	0.026	0.034
c	0.460	0.580	0.018	0.023
D	6.500	6.700	0.256	0.264
D1	5.100	5.460	0.201	0.215
D2	4.830 TYP.		0.190 TYP.	
E	6.000	6.200	0.236	0.244
e	2.186	2.386	0.086	0.094
L	9.800	10.400	0.386	0.409
L1	2.900 TYP.		0.114 TYP.	
L2	1.400	1.700	0.055	0.067
L3	1.600 TYP.		0.063 TYP.	
L4	0.600	1.000	0.024	0.039
Φ	1.100	1.300	0.043	0.051
θ	0°	8°	0°	8°
h	0.000	0.300	0.000	0.012
V	5.350 TYP.		0.211 TYP.	