GOOD-ARK SEMICONDUCTOR

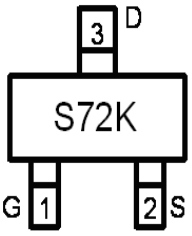
SSF72KB

60V N-Channel MOSFET

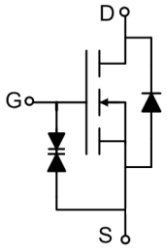
Main Product Characteristics

V_{DSS}	60V
$R_{DS(on)}$	2Ω(max.)
I_D	0.3A

SOT-23



Marking and Pin Assignment



Schematic Diagram

Features and Benefits

- Advanced MOSFET process technology
- Ideal for PWM, load switching and general purpose applications
- Ultra low on-resistance with low gate charge
- Fast switching and reverse body recovery
- ESD Rating: 1000V HBM
- 150 °C operating temperature

Description

The SSF72KB utilizes the latest processing techniques to achieve high cell density, low on-resistance and high repetitive avalanche rating. These features make this device extremely efficient and reliable for use in power switching applications and a wide variety of other applications.

Absolute Max Ratings (T_A=25°C unless otherwise specified)

Symbol	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V①	0.3	A
I_{DM}	Pulsed Drain Current②	1.2	
P_D @T_C = 25°C	Power Dissipation③	0.63	W
V_{DS}	Drain-Source Voltage	60	V
V_{GS}	Gate-to-Source Voltage	± 20	V
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +150	°C

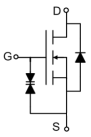
Thermal Resistance

Symbol	Characteristics	Typ.	Max.	Units
$R_{\theta JA}$	Junction-to-ambient (t ≤ 10s) ④	—	200	°C/W

Electrical Characteristics (T_A=25°C unless otherwise specified)

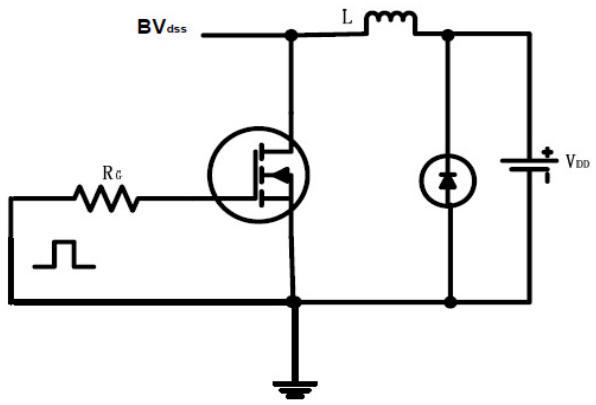
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	60	—	—	V	V_{GS} = 0V, I_D = 250μA
$R_{DS(on)}$	Static Drain-to-Source On-resistance	—	1.5	2	Ω	V_{GS}=10V, I_D=0.5A
		—	—	3		V_{GS}=5V, I_D=0.05A
$V_{GS(th)}$	Gate Threshold Voltage	1.3	—	2.5	V	V_{DS} = V_{GS}, I_D = 250μA
I_{DSS}	Drain-to-Source Leakage Current	—	—	1	μA	V_{DS} = 60V,V_{GS} = 0V
I_{GSS}	Gate-to-Source Forward Leakage	—	—	±100	nA	V_{GS}=±5V,V_{DS}=0V
		—	—	±10	uA	V_{GS}=±20V,V_{DS}=0V
$t_{d(on)}$	Turn-on Delay Time	—	—	25	ns	V_{GS}=10V, VDS=30V, ID=0.2A,R_{GEN}=10Ω
$t_{d(off)}$	Turn-Off Delay Time	—	—	35		
C_{iss}	Input Capacitance	—	40	—	pF	V_{GS} = 0V V_{DS} = 25V f = 1MHz
C_{oss}	Output Capacitance	—	16.6	—		
C_{rss}	Reverse Transfer Capacitance	—	9.5	—		

Source-Drain Ratings and Characteristics

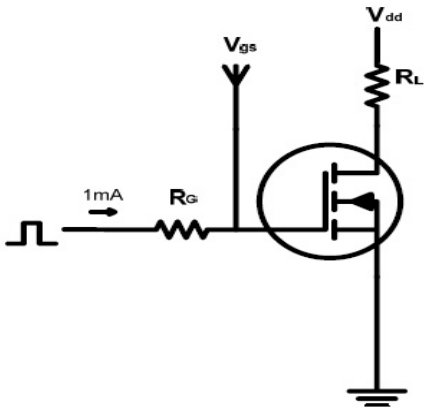
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	0.3	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode)	—	—	1.2	A	
V_{SD}	Diode Forward Voltage	—	—	1.3	V	I_S=0.2A, V_{GS}=0V

Test Circuits and Waveforms

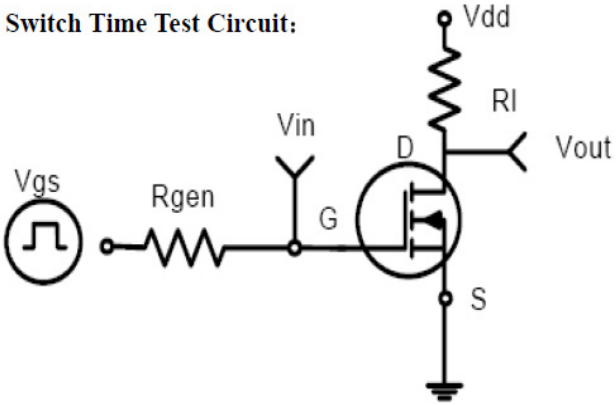
EAS test circuits:



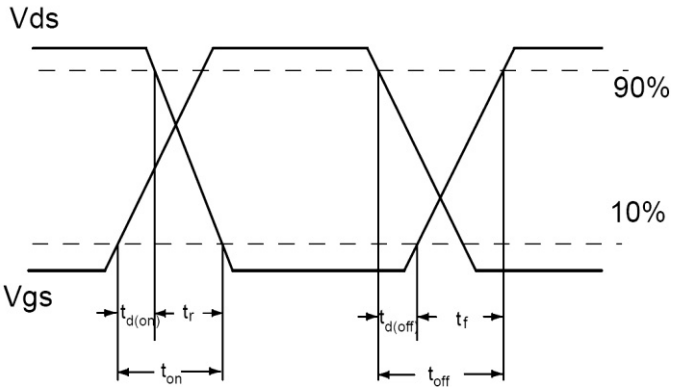
Gate charge test circuit:



Switch Time Test Circuit:



Switching Waveforms:



Notes:

①The maximum current rating is limited by bond-wires.

②Repetitive rating; pulse width limited by max. junction temperature.

③The power dissipation P_D is based on max. junction temperature, using junction-to-case thermal resistance.

④The value of $R_{\theta JA}$ is measured with the device mounted on 1 in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A =25°C

Typical Electrical and Thermal Characteristics

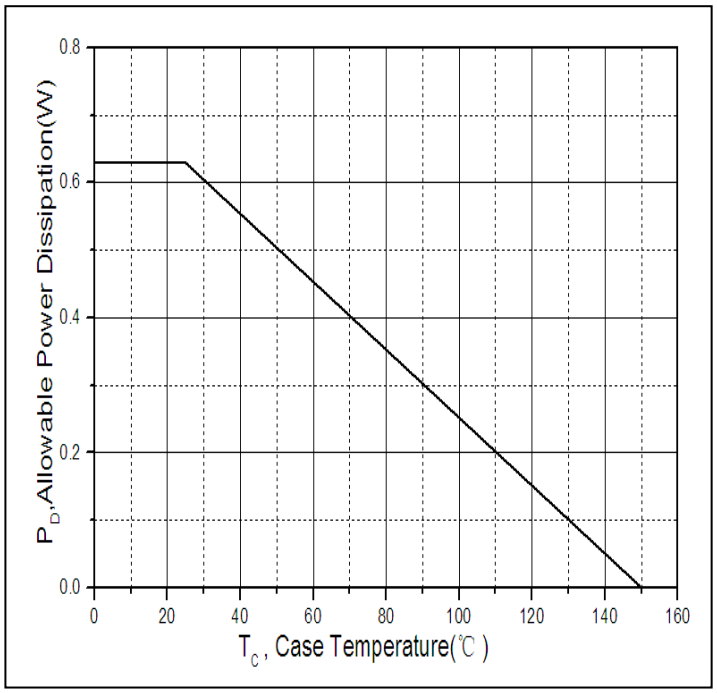


Figure 1. Power Dissipation Vs. Case Temperature

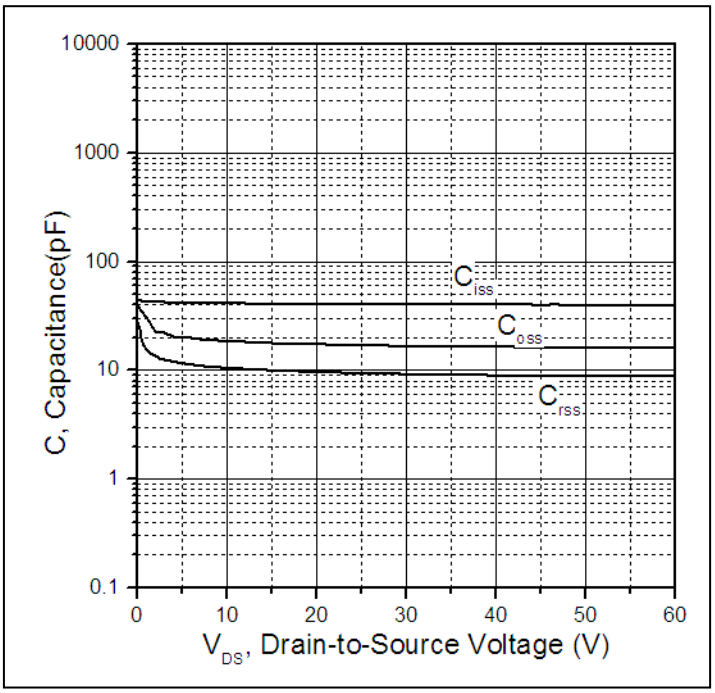


Figure 2.Typical Capacitance Vs. Drain-to-Source Voltage

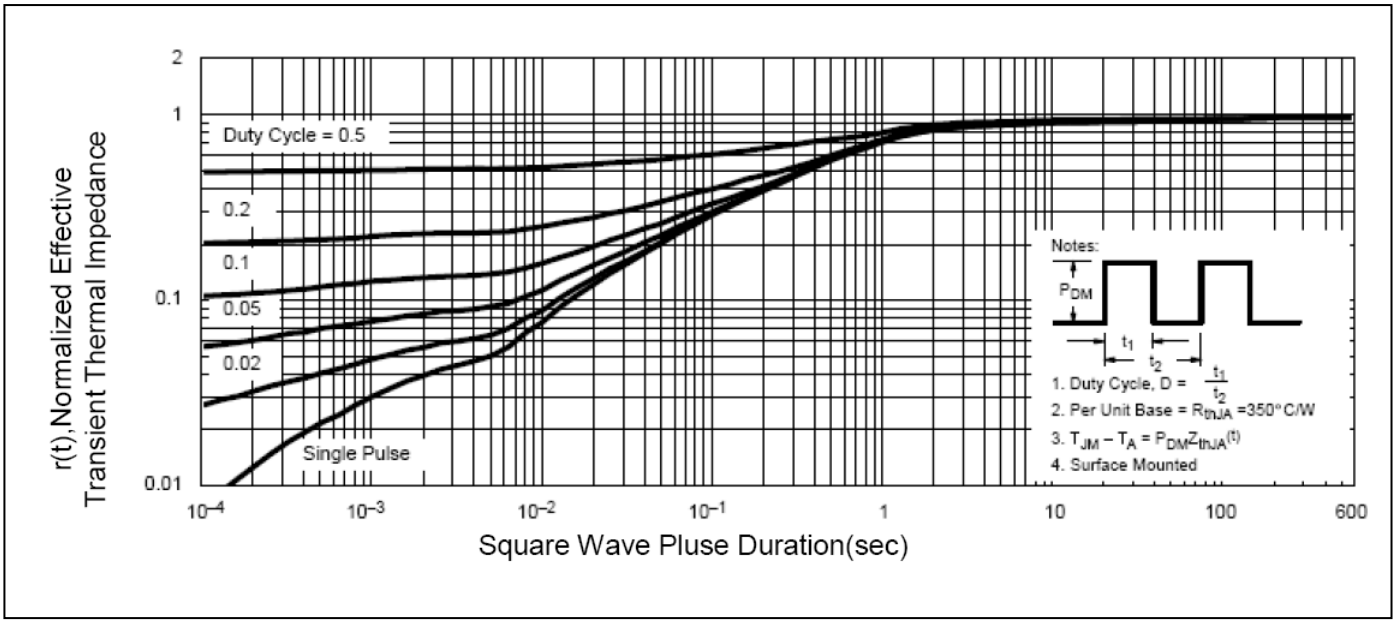
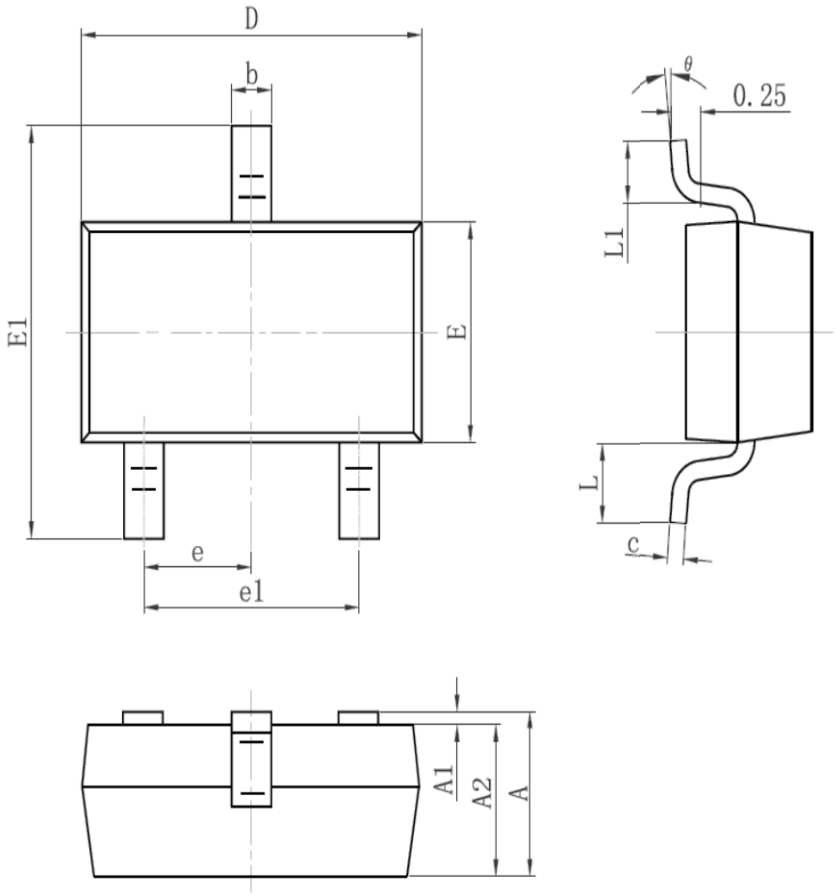


Figure 3. Maximum Effective Transient Thermal Impedance, Junction-to-Case

Mechanical Data

SOT-23 PACKAGE OUTLINE DIMENSION



Symbol	Dimension In Millimeters		Dimension In Inches	
	Min	Max	Min	Max
A	0.900	1.150	0.035	0.045
A1	0.000	0.100	0.000	0.004
A2	0.900	1.050	0.035	0.041
b	0.300	0.500	0.012	0.020
c	0.080	0.150	0.003	0.006
D	2.800	3.000	0.110	0.118
E	1.200	1.400	0.047	0.055
E1	2.250	2.550	0.089	0.100
e	0.95TYP		0.037TYP	
e1	1.800	2.000	0.071	0.079
L	0.55REF		0.022REF	
L1	0.300	0.500	0.012	0.020
θ	0^0	8^0	0^0	8^0

Ordering and Marking Information

Device Marking: S72K

Package (Available)
SOT-23
Operating Temperature Range
C : -55 to 150 ºC

Devices per Unit

Package Type	Units/ Tape	Tapes/Inner Box	Units/Inner Box	Inner Boxes/Carton Box	Units/ Carton Box
SOT-23	3000	10	30000	4	120000

Reliability Test Program

Test Item	Conditions	Duration	Sample Size
High Temperature Reverse Bias(HTRB)	T_j=125°C to 150°C @ 80% of Max $V_{DSS}/V_{CES}/V_R$	168 hours 500 hours 1000 hours	3 lots x 77 devices
High Temperature Gate Bias(HTGB)	T_j=150°C @ 100% of Max V_{GSS}	168 hours 500 hours 1000 hours	3 lots x 77 devices