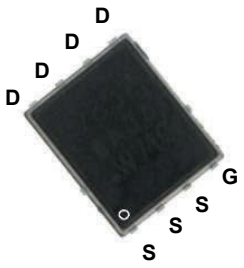
GOOD-ARK SEMICONDUCTOR

GSGP14015

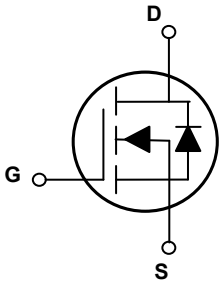
150V N-Channel MOSFET

Main Product Characteristics

$V_{(BR)DSS}$	150V
$R_{DS(ON)}$	14mΩ (Max.)
I_D	100A



PPAK5x6



Schematic Diagram

Features and Benefits

- Advanced MOSFET process technology
- Ideal for high efficiency switched mode power supplies
- Low on-resistance with low gate charge
- Fast switching and reverse body recovery

Description

The GSGP14015 utilizes the latest techniques to achieve high cell density and low on-resistance. These features make this device extremely efficient and reliable for use in high efficiency switch mode power supplies and a wide variety of other applications.

Absolute Maximum Ratings (T_J=25°C unless otherwise specified)

Parameter	Symbol	Parameter	Unit
Drain-Source Voltage	V_{DS}	150	V
Gate-to-Source Voltage	V_{GS}	±20	V
Continuous Drain Current, @ Steady-State (T_C=25°C)	I_D	100	A
Continuous Drain Current, @ Steady-State (T_C=100°C)		63	A
Pulsed Drain Current[2]	I_{DM}	400	A
Power Dissipation (T_C=25°C)[3]	P_D	139	W
		1.1	W/°C
Single Pulse Avalanche Energy[1]	E_{AS}	162	mJ
Single Pulse Avalanche Current	I_{AS}	57	A
Junction-to-Ambient (PCB Mounted, Steady-State)	$R_{\theta JA}$	50	°C/W
Junction-to-Case	$R_{\theta JC}$	0.9	°C/W
Operating Junction and Storage Temperature Range	T_J/T_{STG}	-55 to +150	°C
Soldering Temperature	T_{sold}	260	°C

Electrical Characteristics (T_J=25°C unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
On / Off Characteristics						
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V, I_D=250μA	150	-	-	V
Drain-to-Source Leakage Current	I_{DSS}	V_{DS}=150V, V_{GS}=0V, T_J=25°C	-	-	1.0	μA
		V_{DS}=150V, V_{GS}=0V, T_J=125°C	-	5.0	-	μA
Gate-to-Source Forward Leakage	I_{GSS}	V_{DS}=0V, V_{GS}=20V	-	-	100	nA
		V_{DS}=0V, V_{GS}=-20V	-	-	-100	
Static Drain-to-Source On-Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=50A	-	12.5	14	mΩ
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=250μA	2.0	-	2.4	V
Dynamic and Switching Characteristics						
Input Capacitance	C_{iss}	V_{GS}=0V, V_{DS}=75V, f=1MHz	-	2614	-	pF
Output Capacitance	C_{oss}		-	328	-	
Reverse Transfer Capacitance	C_{rss}		-	15	-	
Total Gate Charge[4,5]	Q_g	I_D=50A, V_{DD}=75V, V_{GS}=10V	-	36	-	nC
Gate-to-Source Charge[4,5]	Q_{gs}		-	24	-	
Gate-to-Drain ("Miller") Charge[4,5]	Q_{gd}		-	4.8	-	
Gate Plateau[4,5]	$V_{plateau}$		-	8.0	-	V
Turn-on Delay Time[4,5]	$t_{d(on)}$	V_{DD}=75V, V_{GS}=10V, R_G=1.6Ω, I_D=50A	-	22	-	nS
Rise Time[4,5]	t_r		-	25	-	
Turn-Off Delay Time Time[4,5]	$t_{d(off)}$		-	25	-	
Fall Time[4,5]	t_f		-	11	-	
Gate Resistance	R_g	f=1MHz	-	1.6	-	Ω
Source-Drain Ratings and Characteristics						
Continuous Source Current (Body Diode)	I_S	MOSFET symbol showing the integral reverse p-n junction diode.	-	-	100	A
Diode Pulse Current	$I_{S.pulse}$		-	-	400	A
Diode Forward Voltage	V_{SD}	I_S=50A, V_{GS}=0V	-	-	1.4	V
Reverse Recovery Time[4]	T_{rr}	I_S=50A, V_{GS}=0V, V_R=48V, dI_F/dt=100A/us	-	96	-	nS
Reverse Recovery Charge[4]	Q_{rr}		-	0.35	-	nC

Notes:

1. EAS test condition: L=0.1mH, V_{DD}=100V, R_G=25Ω.
2. Pulse time of 5μs.
3. The dissipated power value will change with the temperature. When it is greater than 25°C, the dissipated power value will decrease by 1.11°C/W for every 1 degree of temperature increase.
4. Pulse test: Pulse width ≤ 300μs, duty cycle ≤ 2%.
5. Basically unaffected by operating temperature.

Typical Electrical and Thermal Characteristic Curves

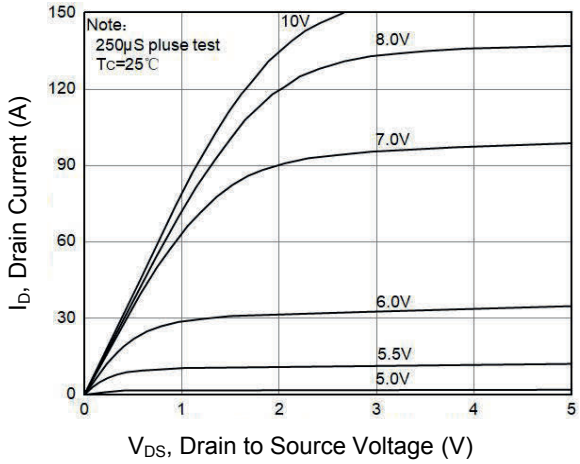


Figure 1. Typical Output Characteristics

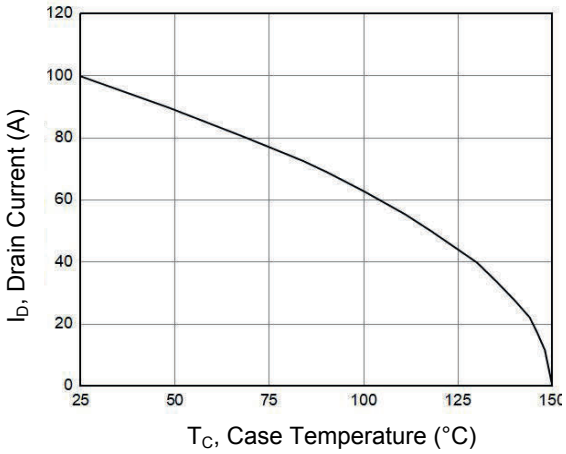


Figure 2. Drain Current vs. T_C

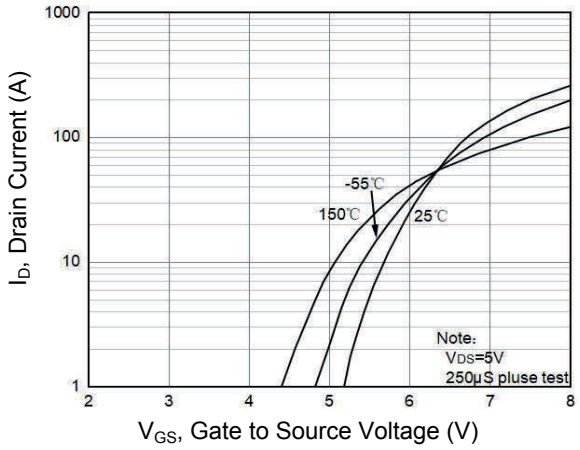


Figure 3. Transfer Characteristics

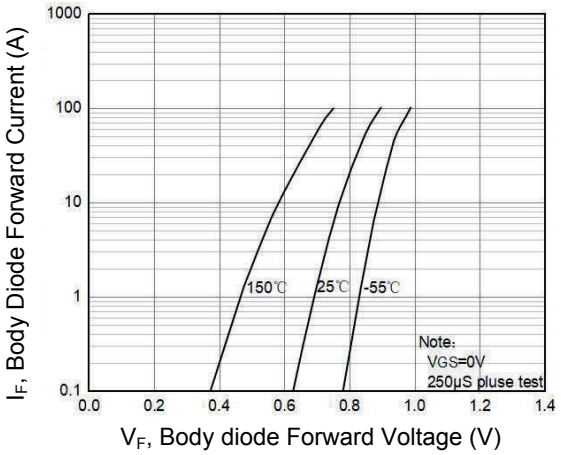


Figure 4. Body Diode Characteristics

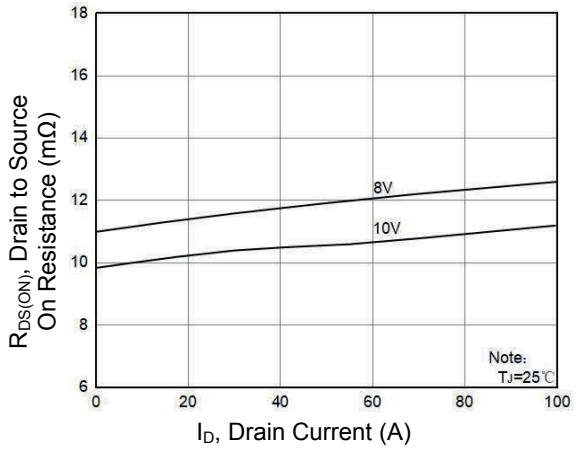


Figure 5. $R_{DS(ON)}$ vs. Drain Current

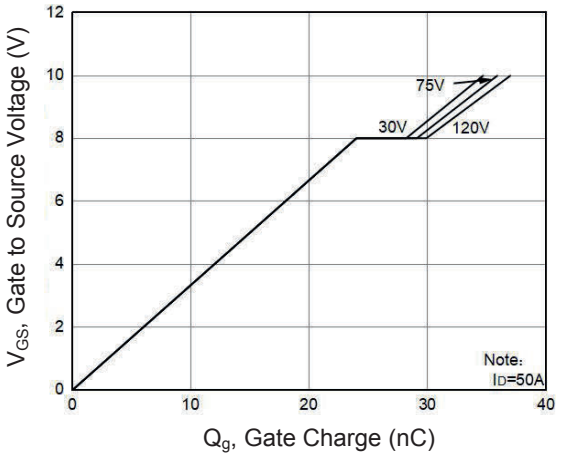


Figure 6. Gate Charge Characteristics

Typical Electrical and Thermal Characteristic Curves

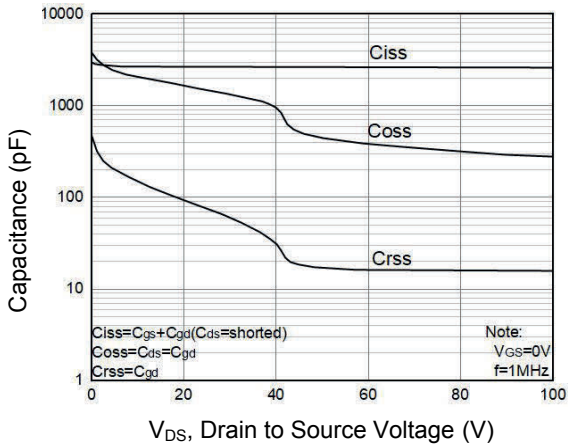


Figure 7. Capacitance Characteristics

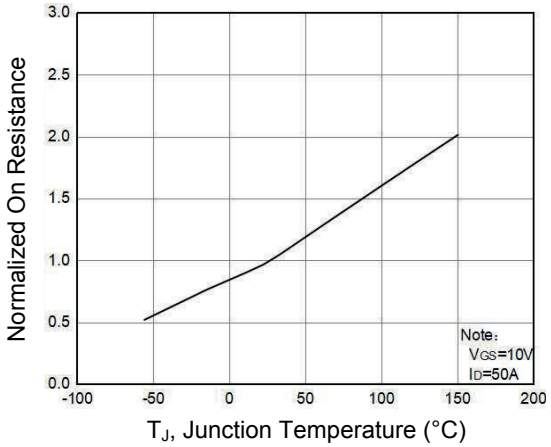


Figure 8. Normalized $R_{DS(ON)}$ vs. T_J

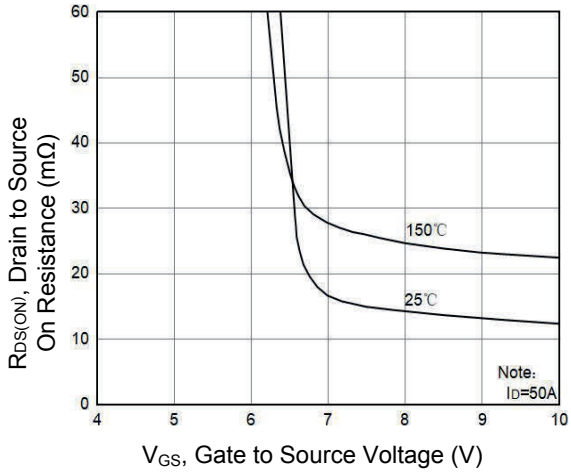


Figure 9. $R_{DS(ON)}$ vs. V_{GS}

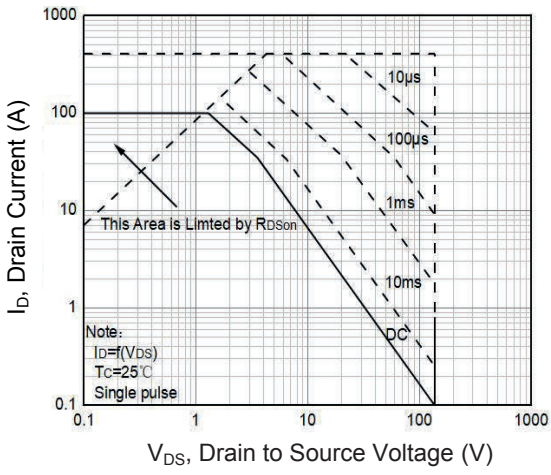


Figure 10. Safe Operation Area

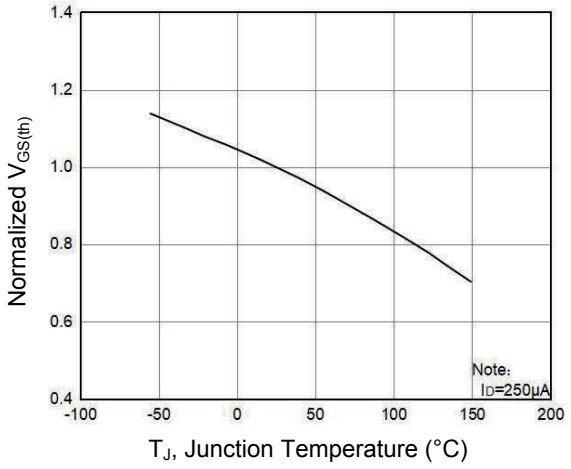


Figure 11. Gate Threshold Voltage vs. T_J

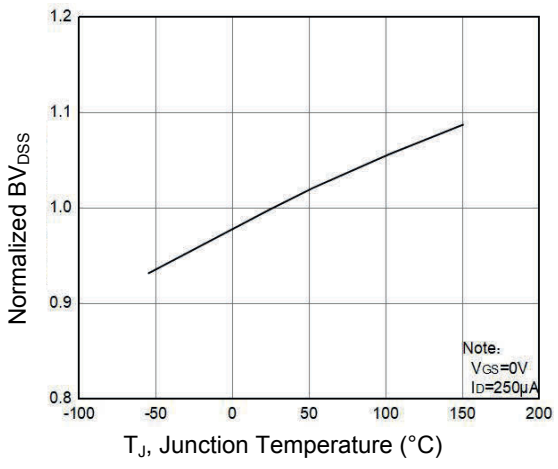
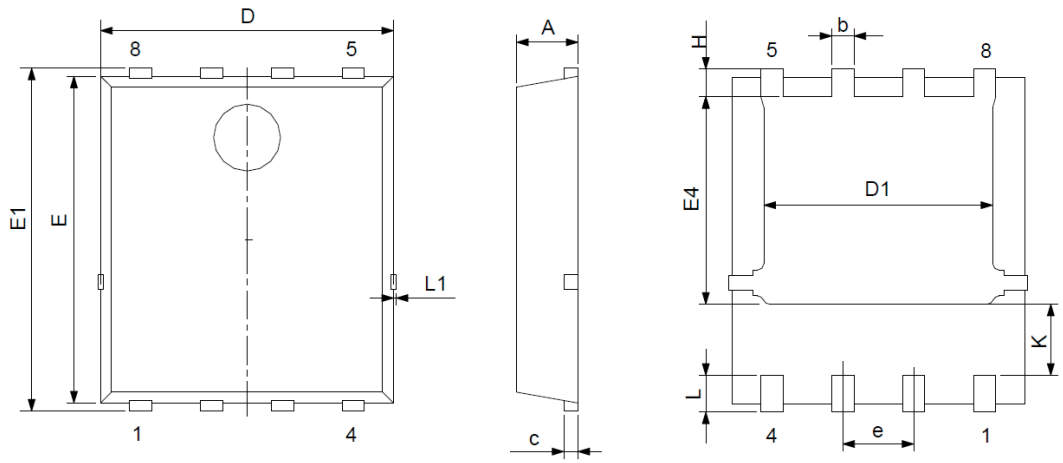


Figure 12. Normalized BV_{DSS} vs. T_J

Package Outline Dimensions (PPAK5x6)



Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	0.900	1.200	0.035	0.047
c	0.154	0.354	0.006	0.014
D	4.800	5.400	0.190	0.213
E	5.660	6.060	0.223	0.240
D1	3.760	4.300	0.148	0.169
E1	5.900	6.350	0.232	0.250
b	0.300	0.550	0.012	0.022
k	1.100	1.500	0.043	0.059
e	1.070	1.370	0.042	0.054
E4	3.340	3.920	0.131	0.154
L	0.300	0.710	0.012	0.028
L1	-	0.120	-	0.005
H	0.400	0.710	0.016	0.028

Order Information

Device	Package	Marking	Carrier	Quantity
GSGP14015	PPAK5x6	P14015	Tape & Reel	5,000pcs / Reel