GOOD-ARK SEMICONDUCTOR

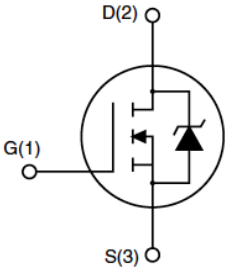
GSFD8005

800V N-Channel MOSFET

Main Product Characteristics

$V_{(BR)DSS}$	800V
$R_{DS(ON)}$	2.7Ω
I_D	5.5A

TO-252 (DPAK)



Schematic Diagram

Features and Benefits

- Advanced MOSFET process technology
- Ideal for high efficiency switched mode power supplies
- Low on-resistance with low gate charge
- Fast switching and reverse body recovery

Description

The GSFD8005 utilizes the latest techniques to achieve high cell density and low on-resistance. These features make this device extremely efficient and reliable for use in high efficiency switch mode power supply and a wide variety of other applications.

Absolute Maximum Ratings (T_C=25°C unless otherwise specified)

Parameter	Symbol	Max.	Unit
Drain-Source Voltage	V_{DS}	800	V
Gate-to-Source Voltage	V_{GS}	± 30	V
Continuous Drain Current, V_{GS} @ 10V [1]	I_D @ T_C = 25°C	5.5	A
Continuous Drain Current, V_{GS} @ 10V [1]	I_D @ T_C = 100°C	3.5	A
Pulsed Drain Current [2]	I_{DM}	22	A
Single Pulse Avalanche Energy @ L=30mH	E_{AS}	323	mJ
Avalanche Current@ L=30mH	I_{AS}	4.5	A
Power Dissipation [3]	P_D @T_C = 25°C	132	W
Linear Derating Factor	$R_{\theta JC}$	1.06	W/°C
Junction-to-Case[3]		0.95	°C/W
Junction-to-Ambient (t ≤ 10s) [4]	$R_{\theta JA}$	62	°C/W
Junction-to-Ambient (PCB Mounted, Steady-State) [4]		45	°C/W
Operating Junction and Storage Temperature Range	T_J T_{STG}	-55 to + 150	°C

Electrical Characteristics (T_C=25°C unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = 250μA	800	-	—	V
Drain-to-Source Leakage Current	I_{DSS}	V_{DS} = 800V, V_{GS} = 0V	-	-	1	μA
		T_J = 125°C	-	-	50	
Gate-to-Source Forward Leakage	I_{GSS}	V_{GS} =30V	-	-	100	nA
		V_{GS} = -30V	-	-	-100	nA
Static Drain-to-Source On-Resistance	$R_{DS(on)}$	V_{GS}=10V, I_D = 2.5A	-	2.1	2.7	Ω
		T_J = 125°C	-	4.4	-	
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250μA	2	3	4	V
		T_J = 125°C	-	1.93	-	
Input Capacitance	C_{iss}	V_{GS} = 0V V_{DS} = 25V f = 1MHz	-	678	-	pF
Output Capacitance	C_{oss}		-	71	-	
Reverse transfer capacitance	C_{rss}		-	4	-	
Total Gate Charge	Q_g	I_D = 5A, V_{DS}=640V, V_{GS} = 10V	-	15.16	-	nC
Gate-to-Source Charge	Q_{gs}		-	4.27	-	
Gate-to-Drain("Miller") Charge	Q_{gd}		-	6.78	-	
Turn-on Delay Time	$t_{d(on)}$	V_{GS}=10V, V_{DS}=400V, R_L=75Ω, R_{GEN}=25Ω I_D=5A	-	11.9	-	nS
Rise Time	t_r		-	23.1	-	
Turn-Off Delay Time	$t_{d(off)}$		-	25.3	-	
Fall Time	t_f		-	24	-	

Source-Drain Ratings and Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Continuous Source Current (Body Diode)	I_S	MOSFET symbol showing the integral reverse p-n junction diode. 	-	-	5.5	A
Pulsed Source Current (Body Diode)	I_{SM}		-	-	22	A
Diode Forward Voltage	V_{SD}	I_S=5A, V_{GS}=0V	-	0.74	1.4	V
Reverse Recovery Time	t_{rr}	T_J = 25°C, IF =5A	-	548	-	ns
Reverse Recovery Charge	Q_{rr}	d_i/d_t=100A/μs	-	2950	-	nC

Notes

1. Calculated continuous current based on maximum allowable junction temperature.
2. Repetitive rating; pulse width limited by max. junction temperature.
3. The power dissipation P_D is based on max. junction temperature, using junction-to-case thermal resistance.
4. The value of $R_{\theta JA}$ is measured with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C

Typical Electrical and Thermal Characteristic Curves

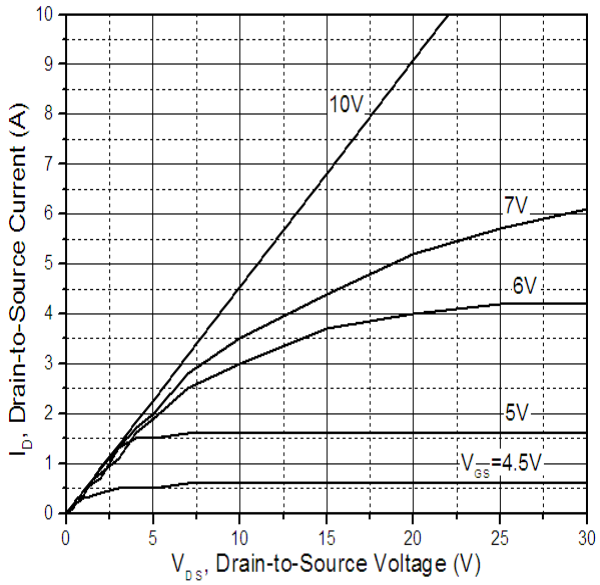


Figure 1. Typical Output Characteristics

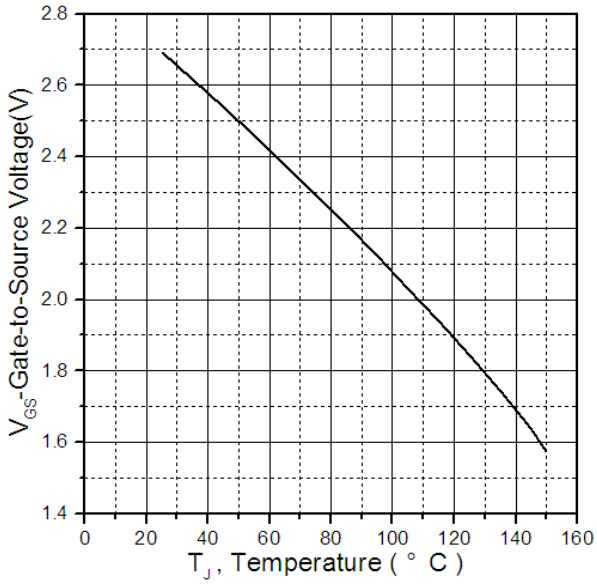


Figure 2. Gate to Source Cut-off Voltage

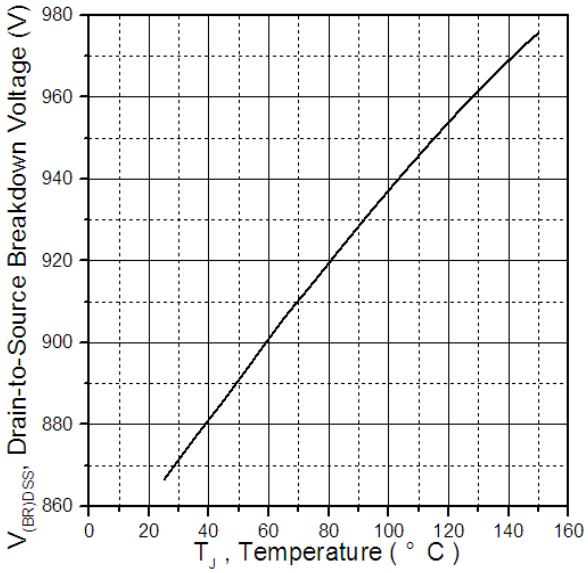


Figure 3. Drain-to-Source Breakdown **Voltage Vs. Case Temperature.**

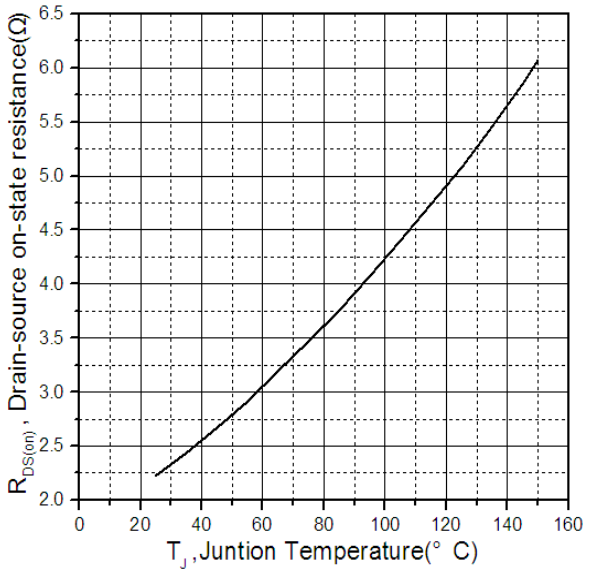


Figure 4. Normalized On-Resistance Vs. Case Temperature

Typical Electrical and Thermal Characteristic Curves

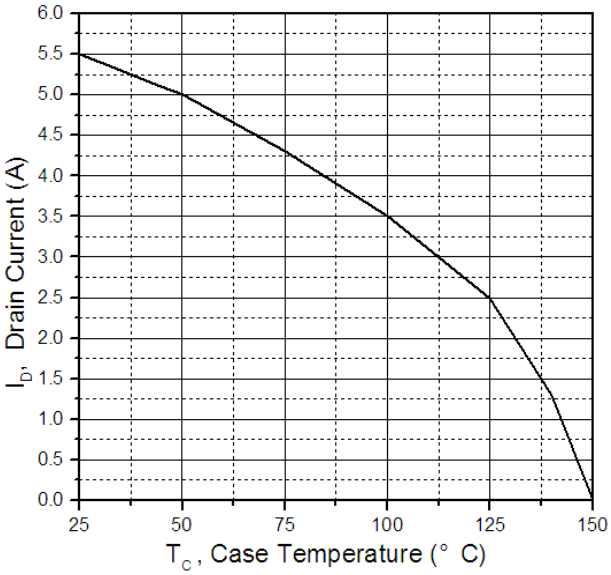


Figure 5. Maximum Drain Current Vs. Case Temperature

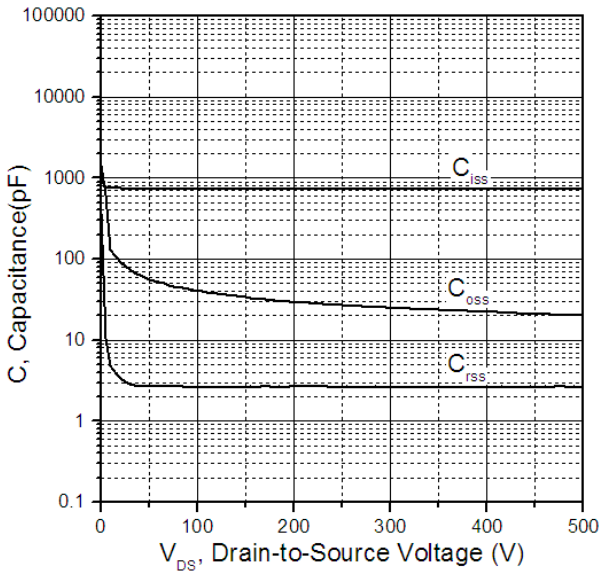


Figure 6. Typical Capacitance Vs. Drain-to- Source Voltage

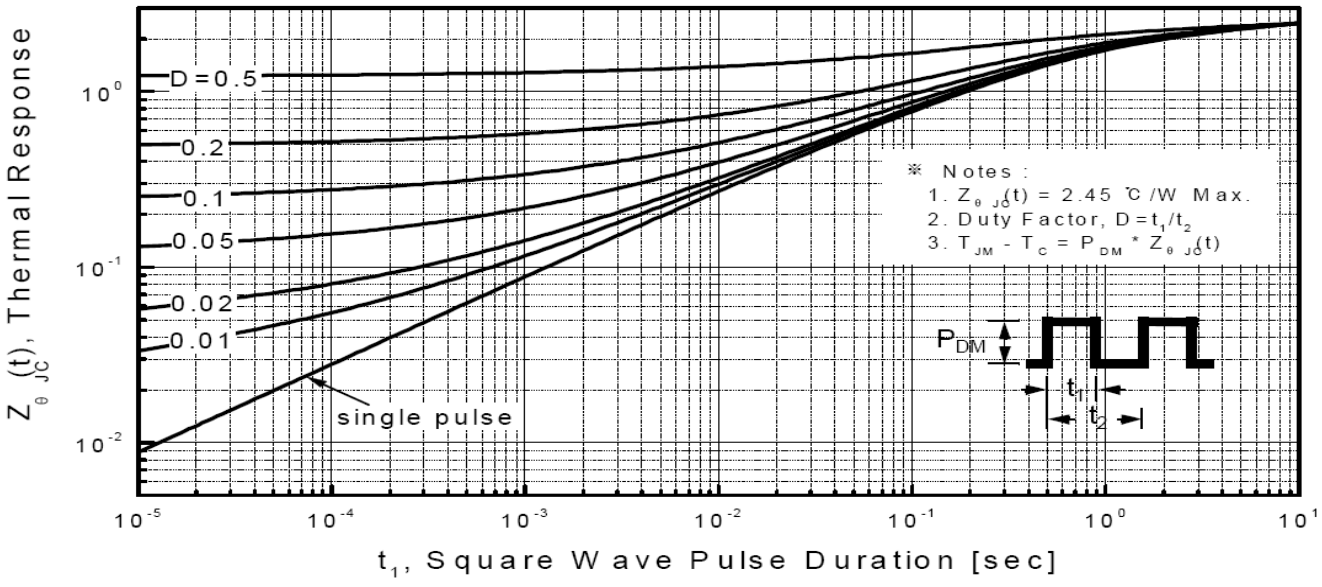


Figure 7. Maximum Effective Transient Thermal Impedance, Junction-to-Case

Test Circuit & Waveform

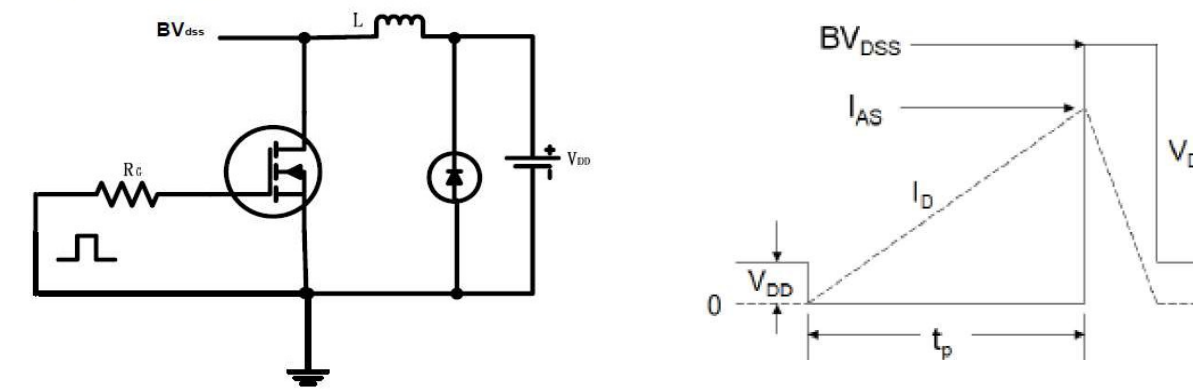


Figure 8. Unclamped Inductive Switching Test Circuit & Waveforms

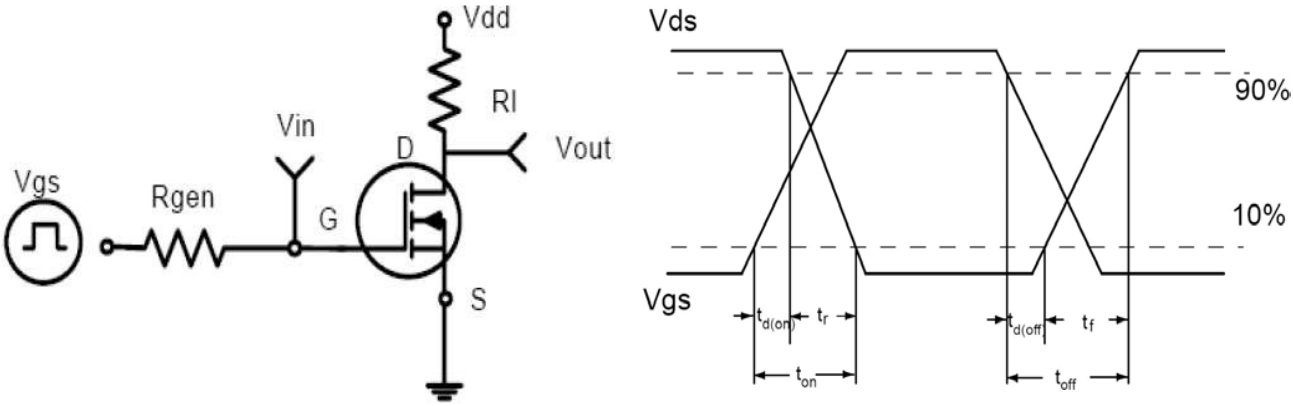


Figure 9. Resistive Switching Test Circuit & Waveforms

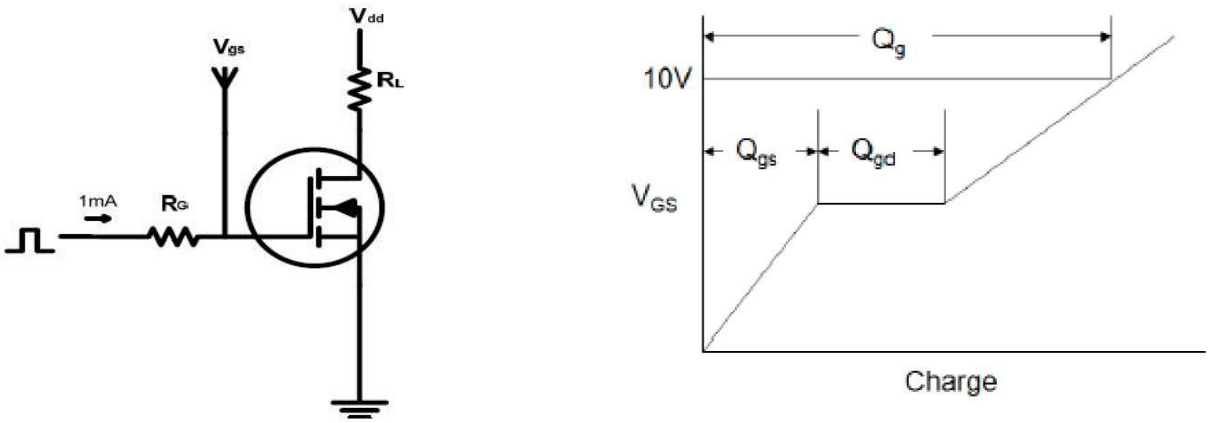
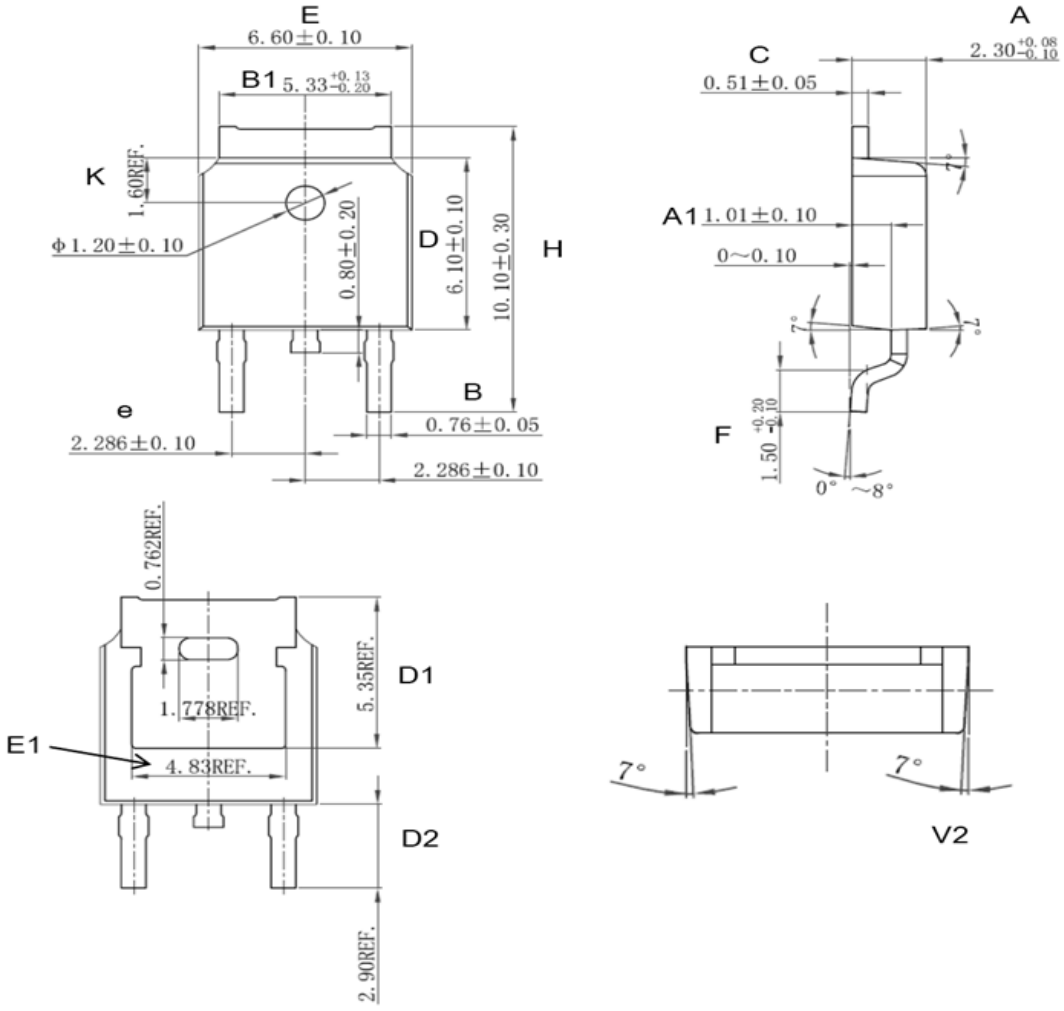


Figure 10. Gate Charge Test Circuit & Waveform

Package Outline Dimensions TO-252 (DPAK)



Symbol	Dimension In Millimeters			Dimension In Inches		
	Min	Nom	Max	Min	Nom	Max
A	2.200	2.300	2.380	0.087	0.091	0.094
A1	0.910	1.010	1.110	0.036	0.040	0.044
B	0.710	0.760	0.810	0.028	0.030	0.032
B1	5.130	5.330	5.460	0.202	0.210	0.215
C	0.460	0.510	0.560	0.018	0.020	0.022
D	6.000	6.100	6.200	0.236	0.240	0.244
D1	5.350 (REF)			0.211 (REF)		
D2	2.900 (REF)			0.114 (REF)		
E	6.500	6.600	6.700	0.256	0.260	0.264
E1	4.83 (REF)			0.190 (REF)		
e	2.186	2.286	2.386	0.086	0.090	0.094
H	9.800	10.100	10.400	0.386	0.398	0.409
F	1.400	1.500	1.700	0.055	0.059	0.067
K	1.600 (REF)			0.063 (REF)		
V2	8^0 (REF)			8^0 (REF)		