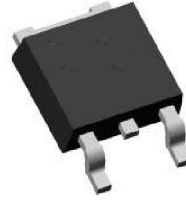
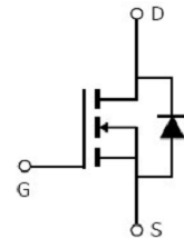


Main Product Characteristics

V_{DSS}	650V
$R_{DS(on)}$	0.30 Ω (typ.)
I_D	11A



TO-252 (DPAK)



Schematic Diagram

Features and Benefits

- High dv/dt and avalanche capabilities
- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance



Description

The GSFD65N11 utilizes the latest techniques to achieve high cell density and low on-resistance. These features make this device extremely efficient and reliable for use in high efficiency switch mode power supply and a wide variety of other applications.

Absolute Maximum Ratings

Parameter	Symbol	Max.	Unit
Continuous Drain Current, $V_{GS} @ 10V$ ①	$I_D @ T_C = 25^\circ C$	11	A
Pulsed Drain Current ②	I_{DM}	33	A
Power Dissipation ③	$P_D @ T_C = 25^\circ C$	83	W
Drain-Source Voltage	V_{DS}	650	V
Gate-to-Source Voltage	V_{GS}	± 30	V
Single Pulse Avalanche Energy	E_{AS}	215	mJ
Avalanche Current	I_{AS}	1.8	A
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 to +150	$^\circ C$
Junction-to-Case ③	$R_{\theta JC}$	1.5	$^\circ C/W$
Junction-to-Ambient ($t \leq 10s$) ④	$R_{\theta JA}$	62	$^\circ C/W$

Electrical Characteristics ($T_C=25^\circ\text{C}$ unless otherwise specified)

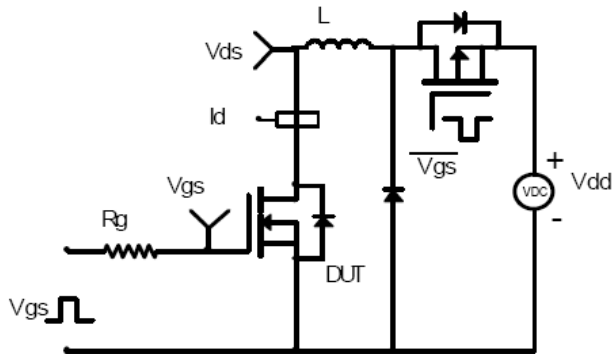
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	650	-	-	V
Static Drain-to-Source On-Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=5.5A$	-	0.30	0.36	Ω
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$	2.5	-	4.5	V
Drain-to-Source Leakage Current	I_{DSS}	$V_{DS}=650V, V_{GS} = 0V$	-	-	1	μA
Gate-to-Source Forward Leakage	I_{GSS}	$V_{GS} = 30V$	-	-	100	nA
		$V_{GS} = -30V$	-	-	-100	
Total Gate Charge	Q_g	$I_D = 11A, V_{DS}=520V, V_{GS} = 10V$	-	22	-	nC
Gate-to-Source Charge	Q_{gs}		-	4	-	
Gate-to-Drain ("Miller") Charge	Q_{gd}		-	8	-	
Turn-on Delay Time	$t_{d(on)}$	$V_{GS}=10V, V_{DS}=400V, R_{GEN}=25\Omega, I_D=11A$	-	70	-	ns
Rise Time	t_r		-	70	-	
Turn-Off Delay Time	$t_{d(off)}$		-	145	-	
Fall Time	t_f		-	59	-	
Input Capacitance	C_{iss}	$V_{GS} = 0V, V_{DS}=100V, f = 1MHz$	-	808	-	pF
Output Capacitance	C_{oss}		-	33	-	
Reverse Transfer Capacitance	C_{rss}		-	2	-	

Source-Drain Ratings and Characteristics

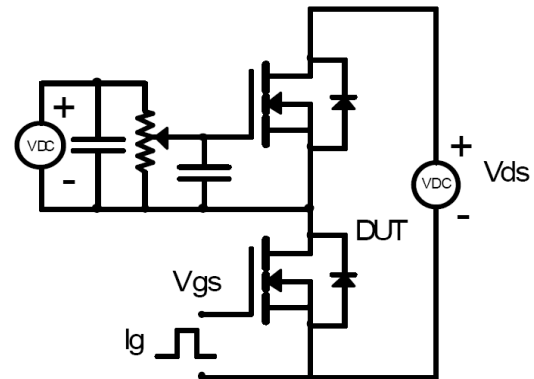
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Continuous Source Current (Body Diode) ①	I_S	MOSFET symbol showing the integral reverse p-n junction diode.	-	-	9.4	A
Pulsed Source Current (Body Diode)	I_{SM}		-	-	33	A
Diode Forward Voltage	V_{SD}	$I_S=5.5A, V_{GS}=0V$	-	0.9	1.2	V
Reverse Recovery Time	t_{rr}	$T_J = 25^\circ\text{C}, I_F = 9.4A, di/dt = 100A/\mu s$	-	377	-	ns
Reverse Recovery Charge	Q_{rr}		-	3400	-	nc

Test Circuits and Waveforms

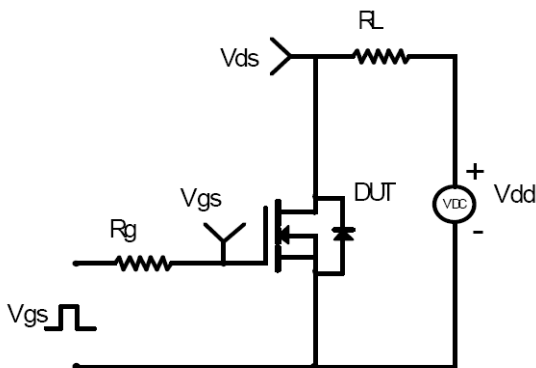
EAS Test Circuit:



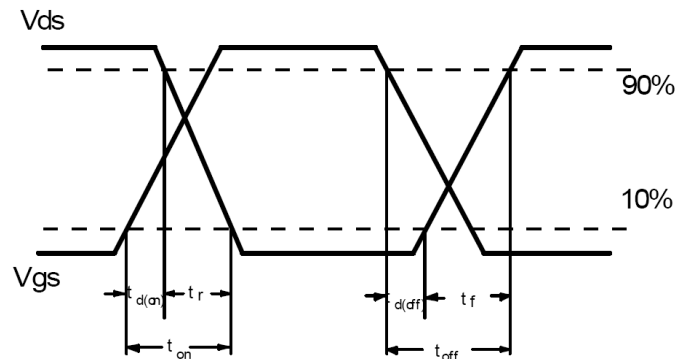
Gate charge test circuit:



Switching Time Test Circuit:



Switching Waveforms:



Notes:

- ① Calculated continuous current based on maximum allowable junction temperature.
- ② Repetitive rating; pulse width limited by max. junction temperature.
- ③ The power dissipation PD is based on max. junction temperature, using junction-to-case thermal resistance.
- ④ The value of $R_{\theta JA}$ is measured with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with $T_A = 25^\circ\text{C}$

Typical Electrical and Thermal Characteristic Curves

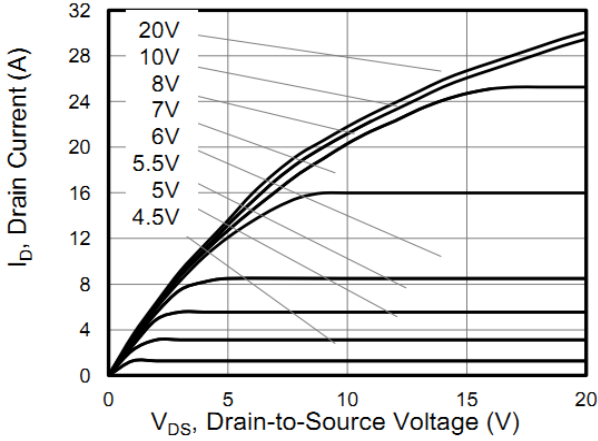


Figure 1. Typical Output Characteristics

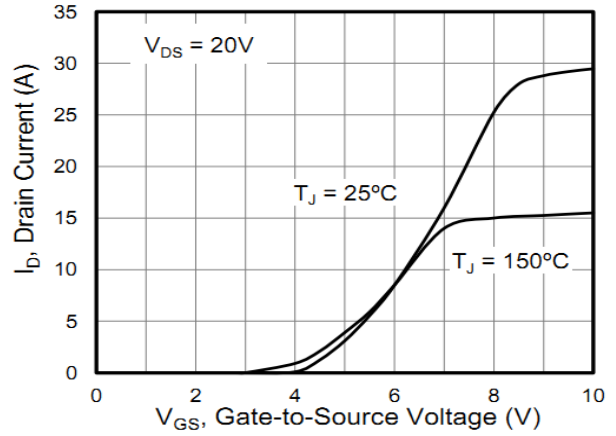


Figure 2. Transfer Characteristics

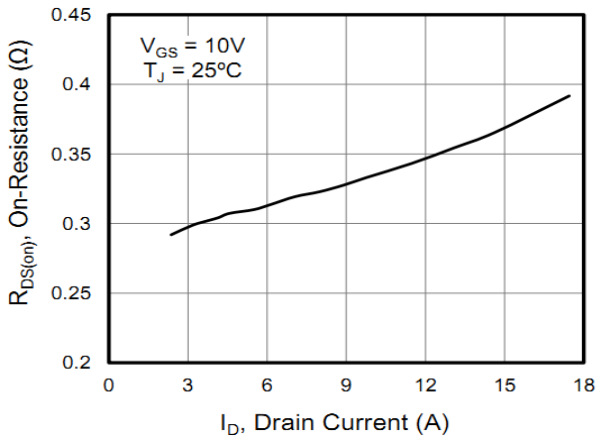


Figure 3. On-Resistance vs. Drain Current

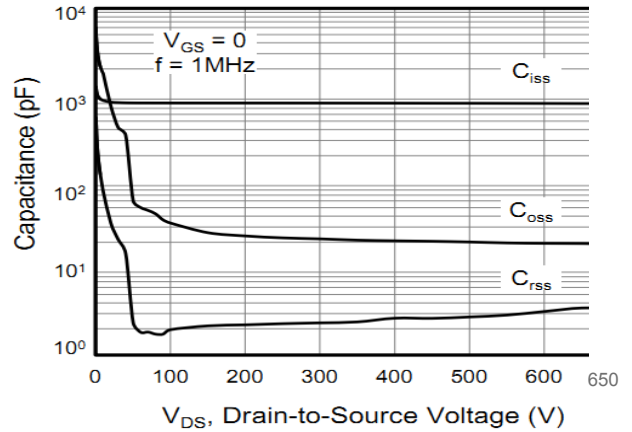


Figure 4. Capacitance

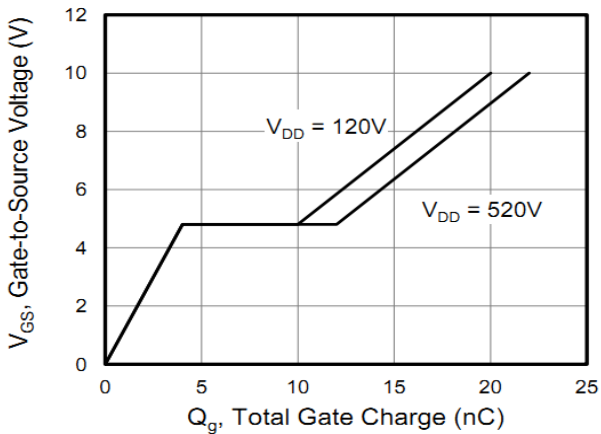


Figure 5. Gate Charge

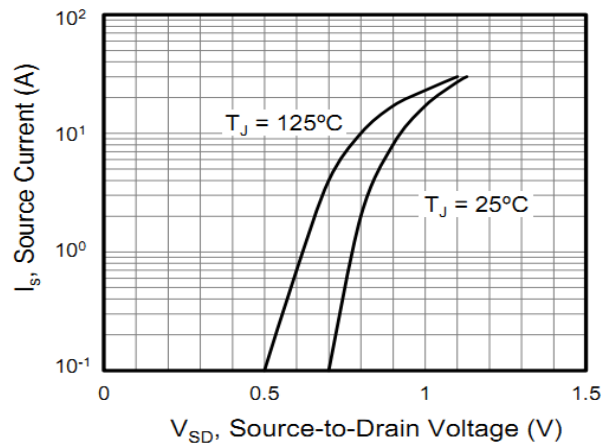


Figure 6. Body Diode Forward Voltage

Typical Electrical and Thermal Characteristic Curves

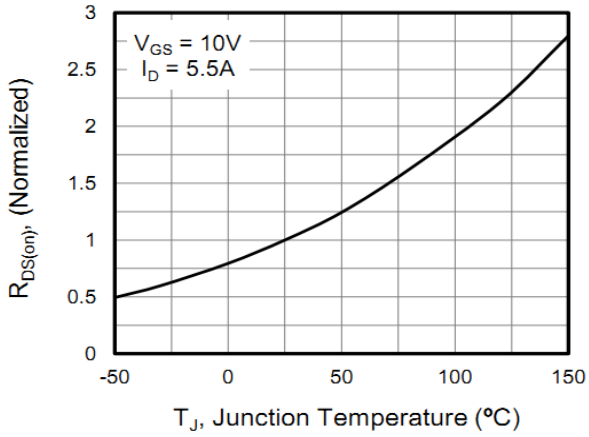


Figure 7. On-Resistance vs. Junction Temperature

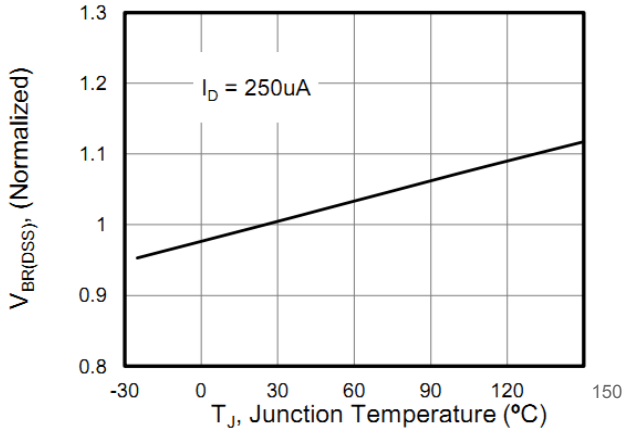


Figure 8. Breakage Voltage vs. Junction Temperature

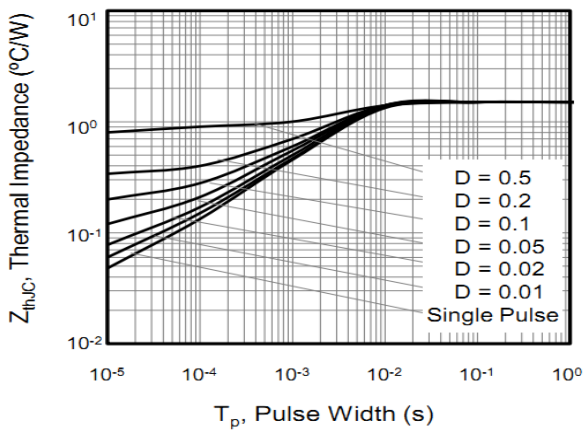


Figure 9. Transient Thermal Impedance

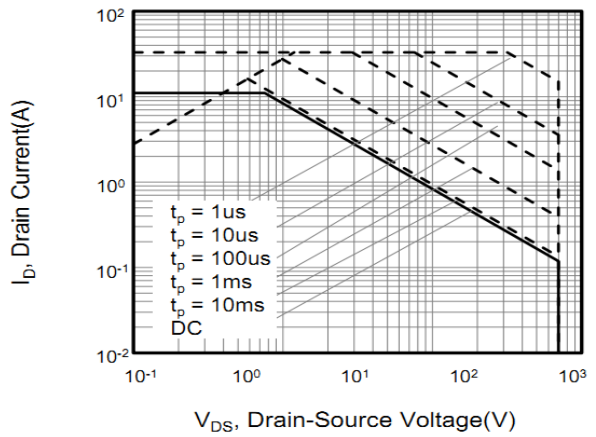


Figure 10. Safe Operation Area

Package Outline Dimensions

TO-252(DPAK)

Dimensions In Millimeters

