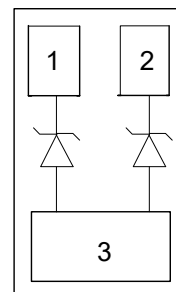


Features

- Ultra small package: 1.0x0.6x0.5mm
- Ultra low capacitance: 0.3pF typical
- Ultra low leakage: nA level
- Operating voltage: 5V
- Low clamping voltage
- 3-pin leadless package
- Complies with following standards:
 - IEC 61000-4-2 (ESD) immunity test Air discharge: $\pm 25\text{kV}$
 - Contact discharge: $\pm 20\text{kV}$
 - IEC 61000-4-5 (Lightning) 5A (8/20 μs)
- RoHS compliant



DFN1006-3L



Schematic Diagram

Applications

- Cellular handsets and accessories
- Display ports
- MDDI ports
- USB 2.0 and 3.0 Ports
- HDMI 1.3 and 1.4
- Digital visual interface (DVI)
- PCI express and serial SATA ports
- Notebook computer
- IEEE 1394

Absolute Maximum Ratings ($T_A=25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Value	Unit
Peak Pulse Power (8/20 μs)	P_{PK}	75	W
Peak Pulse Current (8/20 μs)	I_{PP}	5	A
ESD per IEC 61000-4-2 (Air)	V_{ESD}	± 25	kV
ESD per IEC 61000-4-2 (Contact)		± 20	
Operating Temperature Range	T_J	-55 to +125	$^\circ\text{C}$
Storage Temperature Range	T_{STG}	-55 to +150	$^\circ\text{C}$

Electrical Characteristics ($T_A=25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Reverse Working Voltage	V_{RWM}	Pin 1 or pin 2 to pin 3 and between pin 1 and pin 2	-	-	5	V
Breakdown Voltage	V_{BR}	$I_T=1\text{mA}$, pin 1 or pin 2 to pin 3 and between pin 1 and pin 2	6	-	-	V
Reverse Leakage Current	I_R	$V_{RWM}=5\text{V}$, Pin 1 or pin 2 to pin 3 and between pin 1 and pin 2	-	-	0.5	μA
Clamping Voltage	V_C	$I_{PP}=1\text{A}$ (8 x 20 μs pulse), pin 1 or pin 2 to pin 3	-	-	10	V
		$I_{PP}=5\text{A}$ (8 x 20 μs pulse), pin 1 or pin 2 to pin 3	-	-	15	
Junction Capacitance	C_J	$V_R=0\text{V}$, $f=1\text{MHz}$, between pin 1 and pin 2	-	0.3	0.5	pF
		$V_R=0\text{V}$, $f=1\text{MHz}$, pin 1 or pin 2 to pin 3	-	-	0.8	

Typical Performance Characteristic ($T_A=25^\circ\text{C}$ unless otherwise Specified)

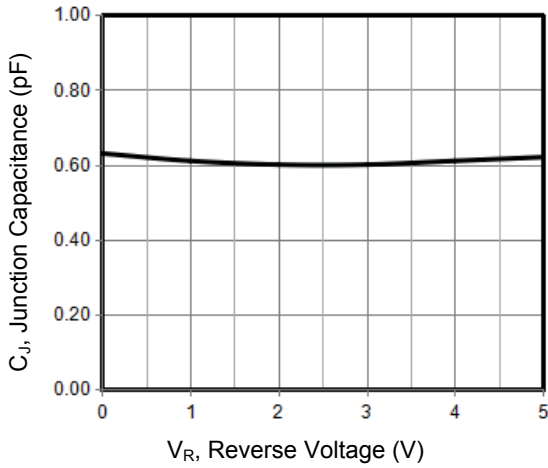


Figure 1. Junction Capacitance vs. Reverse Voltage

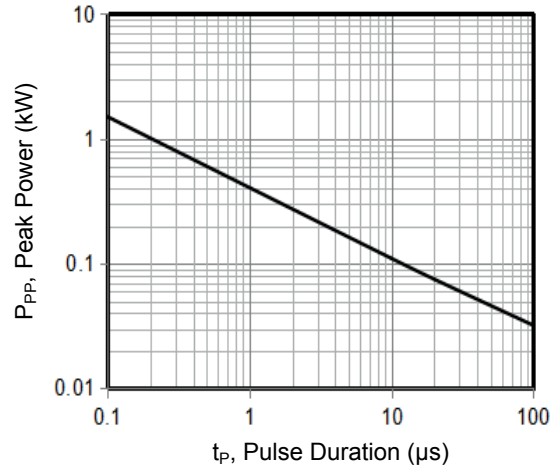


Figure 2. Peak Pulse Power vs. Pulse Time

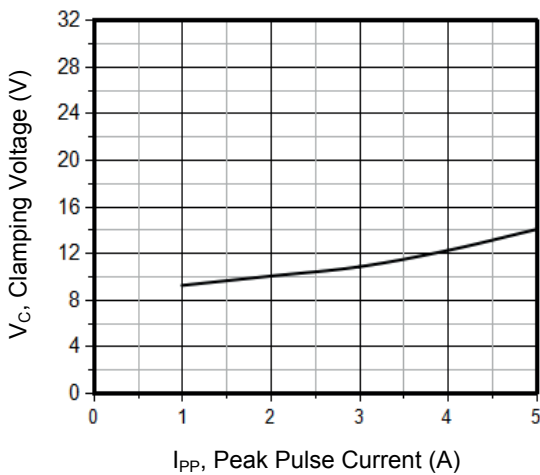


Figure 3. Clamping Voltage vs. Peak Pulse Current

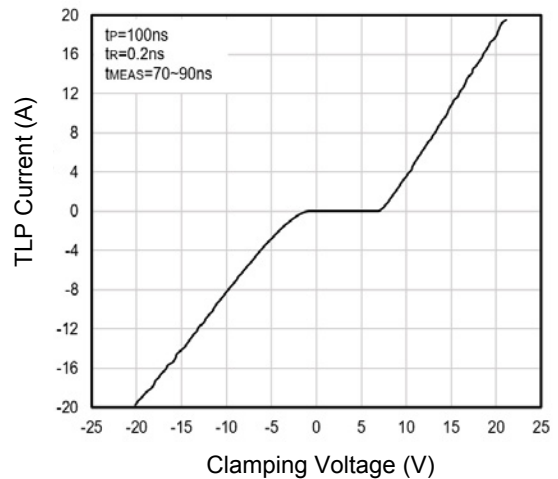


Figure 4. TLP Curve

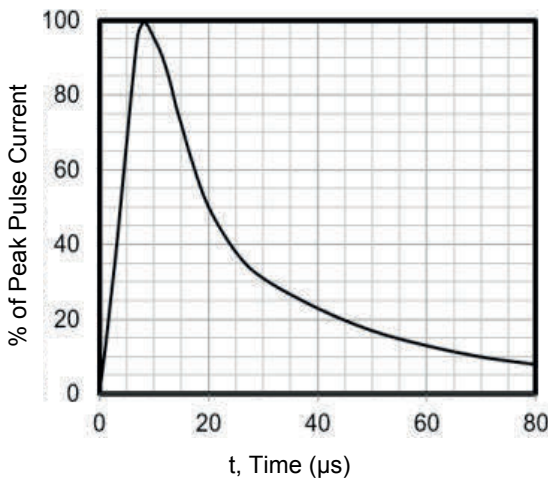


Figure 5. 8 X 20 μs Pulse Waveform

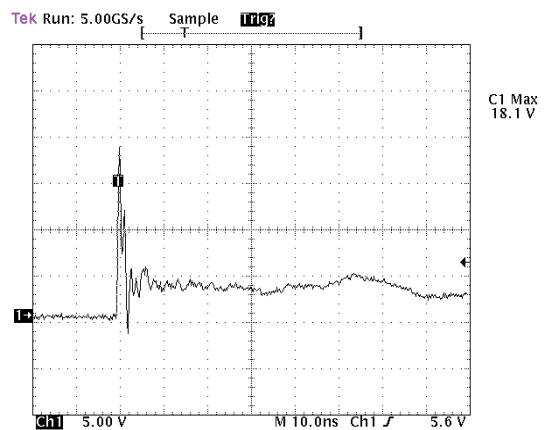
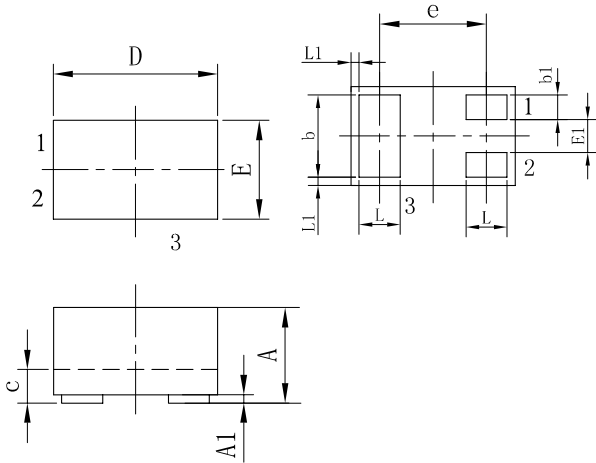


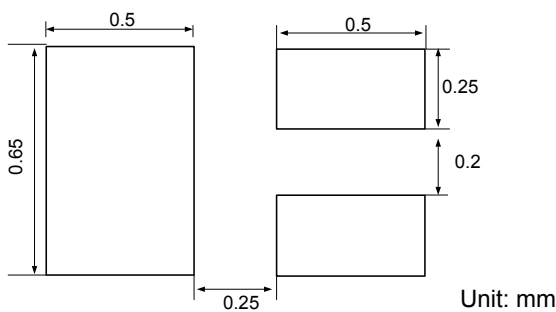
Figure 6. ESD Clamping Voltage
 Note: Data is taken with a 10x attenuator
8 kV Contact per IEC61000-4-2

Package Outline Dimensions (DFN1006-3L)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.45	0.55	0.018	0.022
A1	0.00	0.05	0.000	0.002
b	0.45	0.55	0.018	0.022
b1	0.10	0.20	0.004	0.008
c	0.12	0.18	0.005	0.007
D	0.95	1.05	0.037	0.041
e	0.65 BSC		0.026 BSC	
E	0.55	0.65	0.022	0.026
E1	0.15	0.25	0.006	0.010
L	0.20	0.30	0.008	0.012
L1	0.05 REF		0.002 REF	

Recommended Pad Layout



Order Information

Device	Package	Marking	Carrier	Quantity
GSEZ5U003	DFN1006-3L	52	Tape & Reel	10,000 pcs / Reel

For more information, please contact us at: inquiry@goodarksemi.com