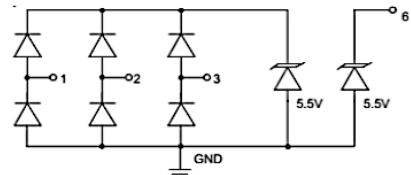
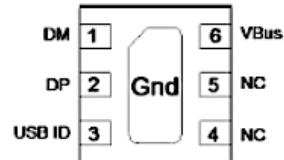


Features

- Low capacitance
- Ultra-low leakage
- Low operating voltage
- Low clamping voltage
- Up to 4 lines and 1 power line protects
- Complies with following standards:
 - IEC 61000-4-2 (ESD) immunity test
 - Air discharge: $\pm 25\text{kV}$
 - Contact discharge: $\pm 20\text{kV}$



Applications

- USB2.0 and USB OTG
- Multi Media Card Interfaces
- SD Card Interfaces
- MDDI Ports and SIM Ports

Absolute Maximum Ratings ($T_A=25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Value	Unit
DP, DM, USB ID (Pins 1, 2, 3)			
Peak Pulse Power (8/20μS)	P_{PK}	60	W
Peak Pulse Current (8/20μS)	I_{PP}	5	A
ESD per IEC 61000-4-2 (Air)	V_{ESD}	± 25	kV
ESD per IEC 61000-4-2 (Contact)		± 20	
IEC 61000-4-4 (EFT) @5/50ns		40	A
Operating Temperature Range	T_J	-55 to +125	°C
Storage Temperature Range	T_{STG}	-55 to +150	°C
VBus (Pin 6)			
Peak Pulse Power (8/20μS)	P_{PK}	75	W
Peak Pulse Current (8/20μS)	I_{PP}	6	A
ESD per IEC 61000-4-2 (Air)	V_{ESD}	± 25	kV
IEC 61000-4-4 (EFT) @5/50ns		40	A
Operating Temperature Range	T_J	-55 to +125	°C
Storage Temperature Range	T_{STG}	-55 to +150	°C

GSEP5U600
Low Capacitance TVS Diode Array

Electrical Characteristics ($T_A=25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
DP, DM, USB ID TVS						
Reverse Working Voltage	V_{RWM}	Pin 1, 2, or 3 to Ground	-	-	5.5	V
Breakdown Voltage	V_{BR}	$I_T = 1\text{mA}$, Pin 6 to Ground	-	-	-	V
Reverse Leakage Current	I_R	$V_{RWM}=5\text{V}$, Pin 6 to Ground	-	-	0.5	uA
Clamping Voltage	V_C	$I_{PP}=1\text{A}$, $T_P=8/20\mu\text{s}$ Any I/O Pin to Ground	-	-	9.5	V
Clamping Voltage	V_C	$I_{PP}=5\text{A}$, $T_P=8/20\mu\text{s}$ Any I/O Pin to Ground	-	-	12	V
Junction Capacitance	C_J	$V_R=0\text{V}$, $f=1\text{MHz}$, Between I/O Pins	-	-	0.4	pF
Junction Capacitance	C_J	$V_R=0\text{V}$, $f=1\text{MHz}$, Any I/O Pin to Ground	-	-	0.8	pF
VBus TVS						
Reverse Working Voltage	V_{RWM}	Pin 6 to Ground	-	-	5.5	V
Breakdown Voltage	V_{BR}	$I_T = 1\text{mA}$, Pin 6 to Ground	6	7	9	V
Reverse Leakage Current	I_R	$V_{RWM}=5.5\text{V}$, Pin 6 to Ground	-	-	3	uA
Clamping Voltage	V_C	$I_{PP}=1\text{A}$ (8X20uS pulse), Pin 6 to Ground	-	-	8	V
Clamping Voltage	V_C	$I_{PP}=8\text{A}$ (8X20uS pulse), Pin 6 to Ground	-	-	12.5	V
Junction Capacitance	C_J	$V_R=0\text{V}$, $f=1\text{MHz}$, Pin 6 to Ground	-	-	60	pF

Typical Performance Characteristics ($T_A=25^\circ\text{C}$ unless otherwise specified)

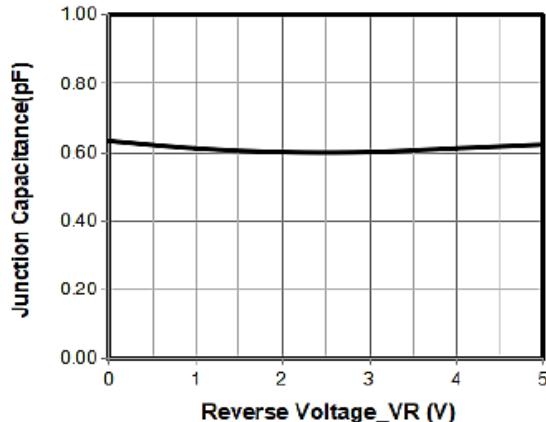


Figure 1. Junction Capacitance vs Reverse Voltage

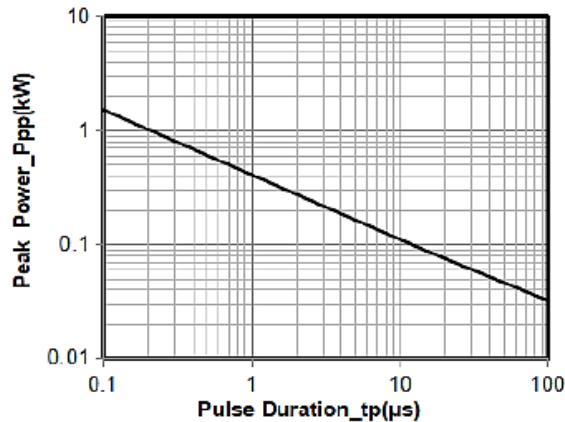


Figure 2. Peak Pulse Power vs Pulse Time

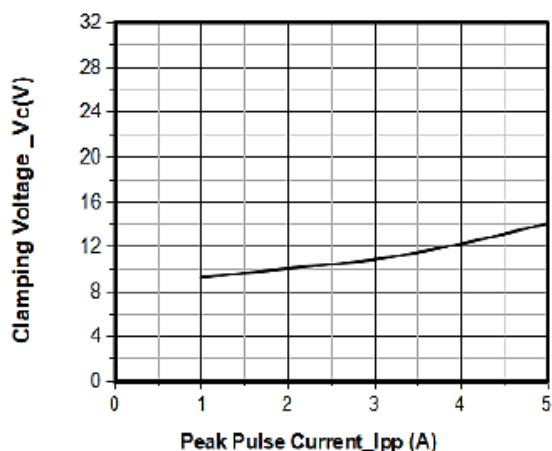


Figure 3. Clamping Voltage vs Peak Pulse Current

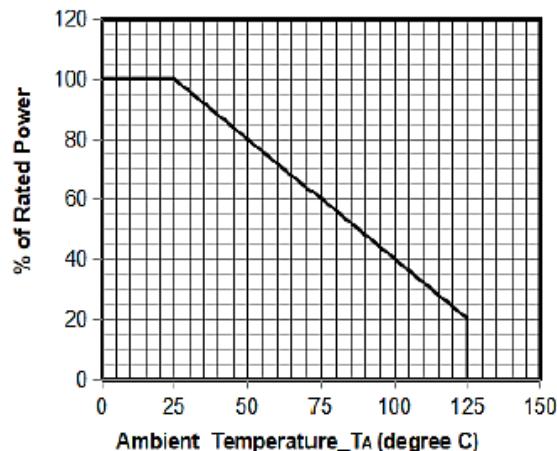


Figure 4. Ambient Temperature vs. % of Rated Power

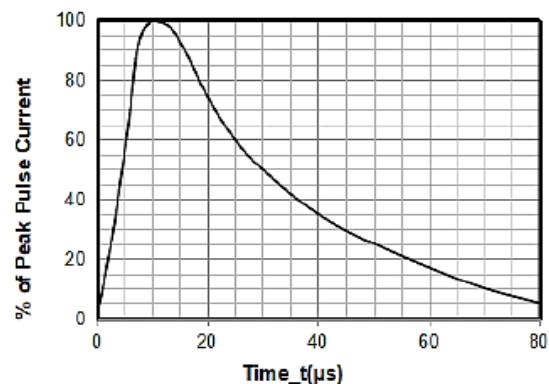
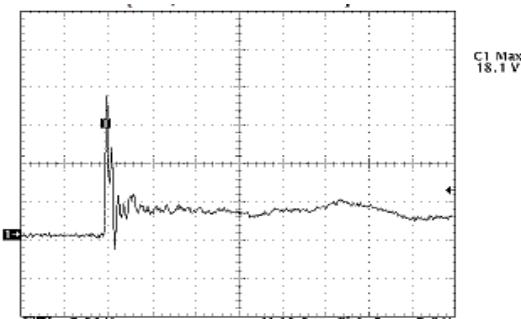


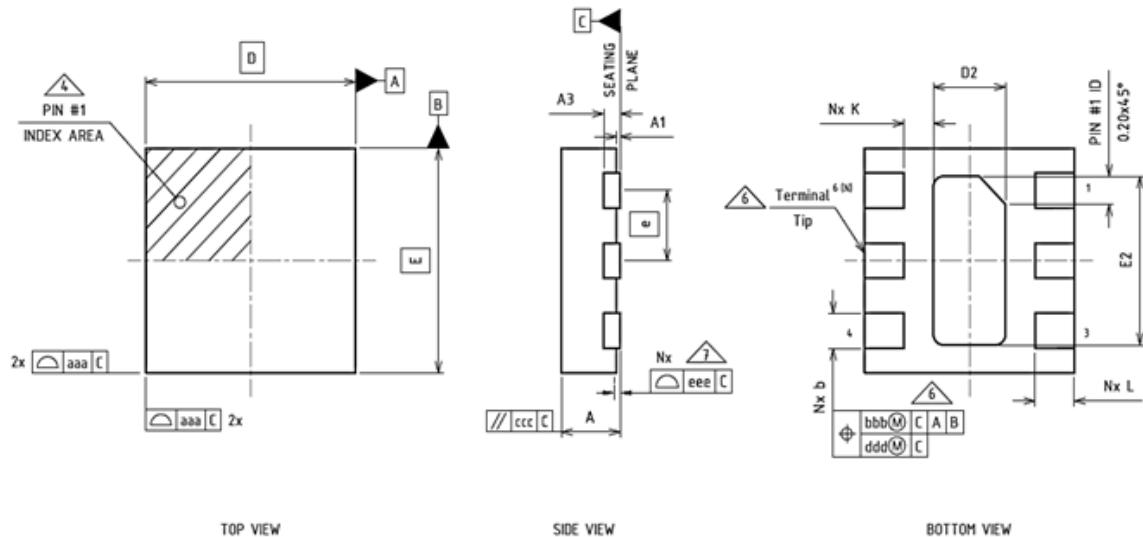
Figure 5. 8x20us Pulse Waveform



Note: Data is taken with a 10x attenuator

Figure 6. ESD Clamping Voltage 8kV Contact per IEC61000-4-2

Package Outline Dimensions DFN1616



TOP VIEW

SIDE VIEW

BOTTOM VIEW

Dimension in millimeters			
Symbols	Min.	Nom.	Max.
A	0.45	0.50	0.55
A1	0.00	0.02	0.05
A3	0.127 Ref		
b	0.18	0.25	0.30
D	1.60 BSC		
E	1.60 BSC		
e	0.50 BSC		
D2	0.40	0.55	0.65
E2	1.05	1.20	1.30
K	0.15		
L	0.20	0.30	0.40
aaa	0.05		
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.08		

Dimension in inches

Symbols	Min.	Nom.	Max.
A	0.018	0.020	0.022
A1	0.000	0.001	0.002
A3	0.005 Ref		
b	0.007	0.010	0.012
D	0.063 BSC		
E	0.063 BSC		
e	0.020 BSC		
D2	0.016	0.022	0.026
E2	0.041	0.047	0.051
K	0.006		
L	0.008	0.012	0.016
aaa	0.002		
bbb	0.004		
ccc	0.004		
ddd	0.002		
eee	0.003		

NOTE:

1. Dimensioning and tolerancing conform to ASME Y14.5-2009.
2. All dimensions are in millimeters.
3. N is the total number of terminals.
4. The location of marked terminal #1 identifier is within the hatched area.
5. NE refers to the maximum number of terminals on E side.
6. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip. If the terminal has a radius on the other end of it, dimension b should not be measured in that radius area.
7. Coplanarity applies to the terminals and all other bottom surface metalization.

Suggested Pad Layout

