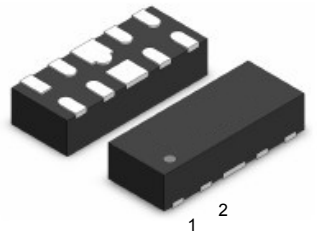
GOOD-ARK SEMICONDUCTOR

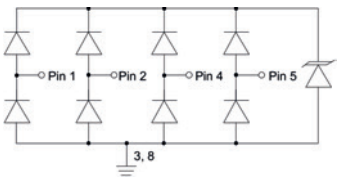
GSECL3U0021
Ultra Low Capacitance ESD TVS Array

Features

- Ultra low capacitance: 0.2pF typical (I/O to I/O)
- Ultra low leakage: nA level
- Operating voltage: 3.3V
- Low clamping voltage
- Complies with following standards:
  -IEC 61000-4-2 (ESD) immunity test
  Air discharge: ±25kV
  Contact discharge: ±15kV
  -IEC61000-4-5 (Lightning) 6A (8/20μs)
- RoHS compliant



DFN2510



Schematic Diagram

Applications

- Display ports
- MDDI / MHL
- Thunderbolt
- USB 3.0 / USB 3.1
- Digital visual interface (DVI)
- PCI express and serial SATA ports

Absolute Maximum Ratings (T_A=25°C unless otherwise specified)

Parameter	Symbol	Value	Unit
Peak Pulse Power (8/20μs)	P_{PK}	24	W
Peak Pulse Current (8/20μs)	I_{PP}	6	A
ESD per IEC 61000−4−2 (Air)	V_{ESD}	±25	kV
ESD per IEC 61000−4−2 (Contact)		±15	
Operating Temperature Range	T_J	−55 to +125	°C
Storage Temperature Range	T_{STG}	−55 to +150	°C

Electrical Characteristics (T_A=25°C unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Reverse Working Voltage	V_{RWM}	Any I/O pin to ground	-	-	3.3	V
Breakdown Voltage	V_{BR}	I_T=1mA, any I/O pin to ground	3.5	-	-	V
Reverse Leakage Current	I_R	V_{RWM}=3.3V, any I/O pin to ground	-	-	0.2	μA
Clamping Voltage	V_C	I_{PP}=6A (8 x 20μs pulse), any I/O pin to ground	-	-	4	V
ESD Clamping Voltage[1]	V_C	I_{PP}=4A, t_p=0.2/100ns (TLP), any I/O pin to ground	-	2.8	-	V
		I_{PP}=16A, t_p=0.2/100ns (TLP), any I/O pin to ground	-	5.1	-	V
Dynamic Resistance[2]	R_{DYN}	t_p=0.2/100ns (TLP), any I/O pin to ground	-	0.19	-	Ohm
Junction Capacitance	C_J	$V_{pin3,8}$=0V, V_{in}=1.0V, f=1MHz, any I/O pin to ground	-	0.4	0.6	pF
Junction Capacitance	C_J	$V_{pin3,8}$=0V, V_{in}=1.0V, f=1MHz, any I/O pin to ground	-	0.2	0.3	pF

Note:

1. Transmission line pulse test (TLP) settings: t_p=100ns, t_r=0.2ns.
2. Dynamic resistance calculated from ITLP=4A to ITLP=16A.

Typical Performance Characteristics (T_A=25°C unless otherwise Specified)

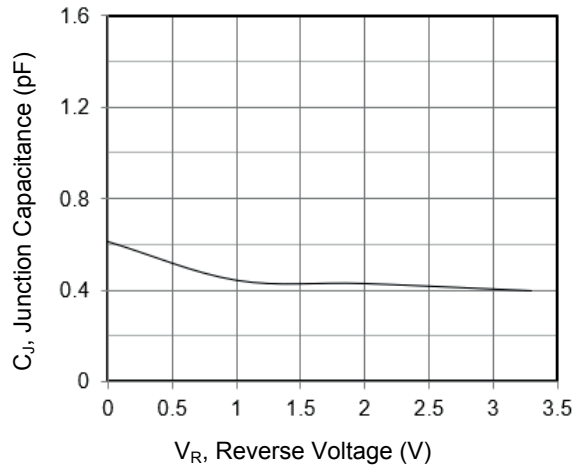


Figure 1. Junction Capacitance vs. Reverse Voltage

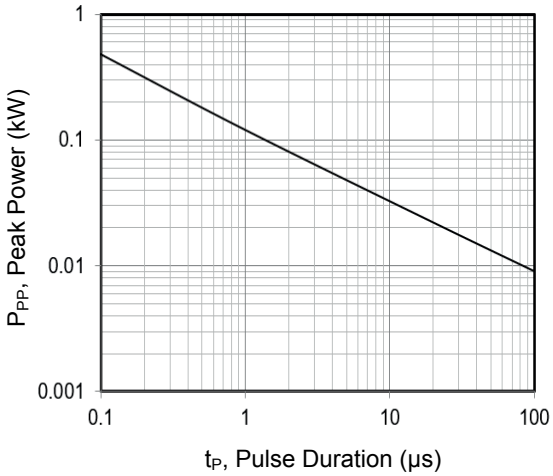


Figure 2. Peak Pulse Power vs. Pulse Time

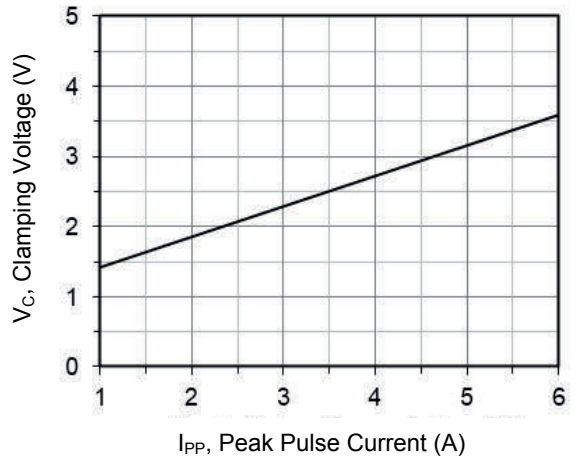


Figure 3. Clamping Voltage vs. Peak Pulse Current (t_p=8/20μs)

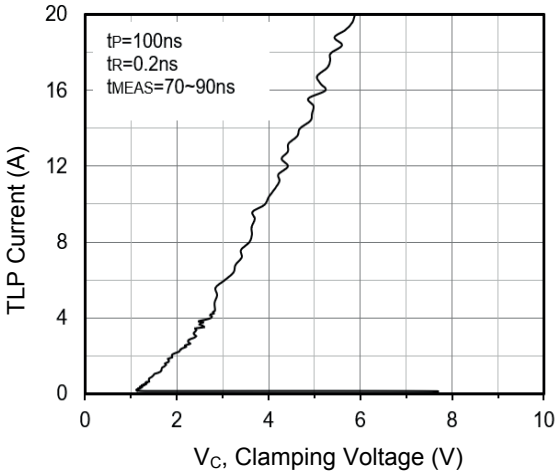


Figure 4. TLP Measurement

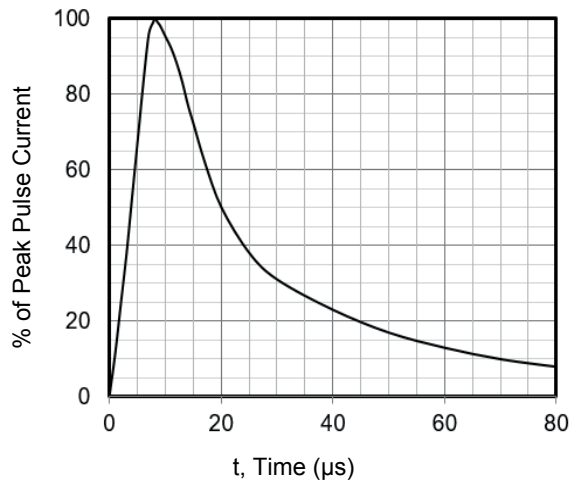


Figure 5. 8 X 20μs Pulse Waveform

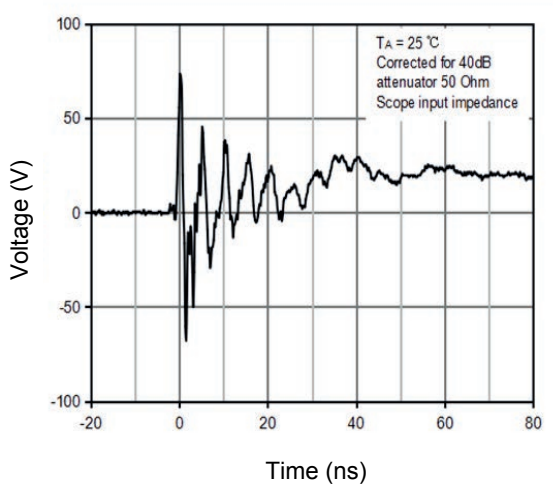
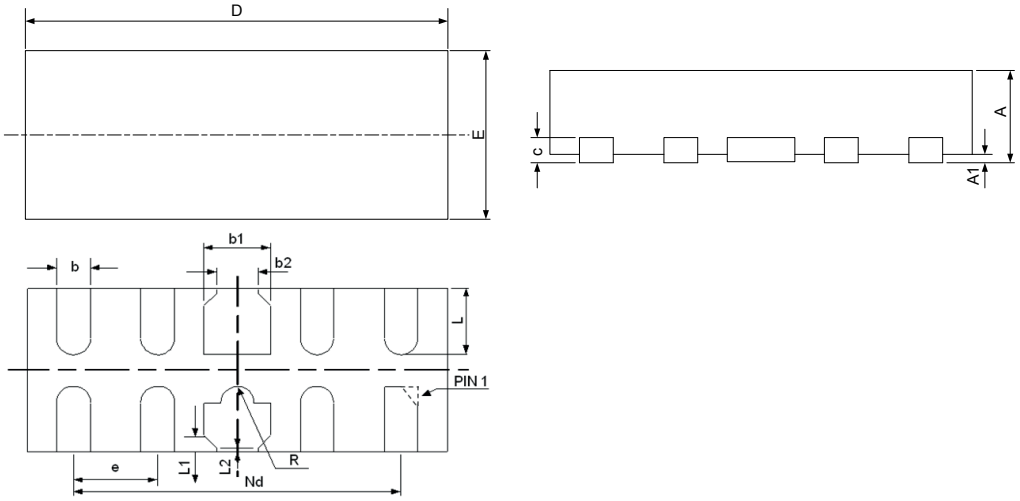


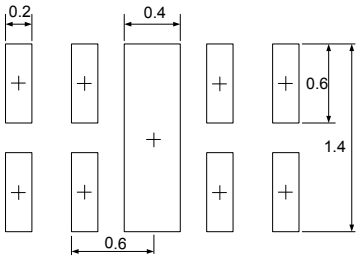
Figure 6. ESD Clamping Voltage 8 kV Contact per IEC61000−4−2

Package Outline Dimensions (DFN2510)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.450	0.600	0.018	0.024
A1	0.000	0.050	0.000	0.002
b	0.150	0.250	0.006	0.010
b1	0.350	0.450	0.014	0.018
b2	0.200	0.300	0.008	0.012
c	0.100	0.200	0.004	0.008
D	2.450	2.550	0.096	0.100
e	0.50BSC		0.020BSC	
Nd	2.00BSC		0.080BSC	
E	0.950	1.050	0.037	0.041
L	0.330	0.450	0.013	0.018
L1	0.075REF		0.003REF	
L2	0.050REF		0.002REF	
R	0.050	0.150	0.002	0.006

Recommended Pad Layout



unit: mm

Order Information

Device	Package	Marking	Carrier	Quantity
GSECL3U0021	DFN2510	3345C	Tape & Reel	3,000pcs / Reel

For more information, please contact us at: inquiry@goodarksemi.com