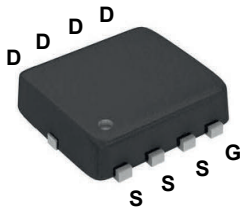
GSGN2R104AU

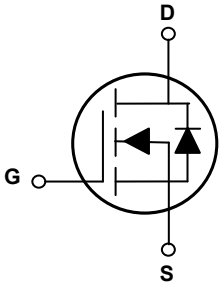
40V N-Channel MOSFET

Main Product Characteristics

$V_{(BR)DSS}$	40V
$R_{DS(ON)}$	2.1mΩ (Max.)
I_D	129A



PPAK3x3



Schematic Diagram

Features and Benefits

- Advanced MOSFET process technology
- Ideal for high efficiency switched mode power supplies
- Low on-resistance with low gate charge
- Fast switching and reverse body recovery
- AEC-Q101 qualified

Description

The GSGN2R104AU utilizes the latest techniques to achieve high cell density and low on-resistance. These features make this device extremely efficient and reliable for use in high efficiency switch mode power supplies and a wide variety of other applications.

Absolute Maximum Ratings (T_J=25°C unless otherwise specified)

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	40	V
Gate-to-Source Voltage	V_{GS}	±20	V
Continuous Drain Current, @ Steady-State (T_C=25°C)	I_D	129	A
Continuous Drain Current, @ Steady-State (T_C=100°C)		81	A
Pulsed Drain Current[2]	I_{DM}	516	A
Power Dissipation (T_C=25°C)[3]	P_D	76	W
		0.51	W/°C
Single Pulse Avalanche Energy[1]	E_{AS}	105	mJ
Single Pulse Avalanche Current	I_{AS}	46	A
Thermal Resistance, Junction-to-Ambient (PCB Mounted, Steady-State)	$R_{\theta JA}$	50	°C/W
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	1.97	°C/W
Operating Junction and Storage Temperature Range	T_J/T_{STG}	-55 to +175	°C
Soldering Temperature	T_{sold}	260	°C

Electrical Characteristics (T_J=25°C unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
On / Off Characteristics						
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V, I_D=250μA	40	-	-	V
Drain-to-Source Leakage Current	I_{DSS}	V_{DS}=40V, V_{GS}=0V, T_J=25°C	-	-	1.0	μA
		V_{DS}=40V, V_{GS}=0V, T_J=125°C	-	1.0	-	μA
Gate-to-Source Forward Leakage	I_{GSS}	V_{DS}=0V, V_{GS}=20V	-	-	100	nA
		V_{DS}=0V, V_{GS}=-20V	-	-	-100	
Static Drain-to-Source On-Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=20A	-	1.6	2.1	mΩ
		V_{GS}=4.5V, I_D=15A	-	2.8	3.5	
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=250μA	1.2	-	2.6	V
Dynamic and Switching Characteristics						
Input Capacitance	C_{iss}	V_{GS}=0V, V_{DS}=25V, f=1MHz	-	2612	-	pF
Output Capacitance	C_{oss}		-	926	-	
Reverse Transfer Capacitance	C_{rss}		-	42	-	
Total Gate Charge[4,5]	Q_g	I_D=50A, V_{DD}=20V, V_{GS}=10V	-	43	-	nC
Gate-to-Source Charge[4,5]	Q_{gs}		-	13	-	
Gate-to-Drain ("Miller") Charge[4,5]	Q_{gd}		-	6.4	-	
Gate Plateau[4,5]	$V_{plateau}$		-	4.6	-	V
Turn-On Delay Time[4,5]	$t_{d(on)}$	V_{DD}=20V, V_{GS}=10V, R_G=4.7Ω, I_D=50A	-	12	-	nS
Rise Time[4,5]	t_r		-	56	-	
Turn-Off Delay Time[4,5]	$t_{d(off)}$		-	42	-	
Fall Time[4,5]	t_f		-	12	-	
Gate Resistance	R_g	f=1MHz	-	1.1	-	Ω
Drain-Source Ratings and Characteristics						
Continuous Source Current (Body Diode)	I_S	MOSFET symbol showing the integral reverse p-n junction diode.	-	-	129	A
Diode Pulse Current	$I_{S.pulse}$		-	-	516	A
Diode Forward Voltage	V_{SD}	I_S=50A, V_{GS}=0V	-	-	1.4	V
Reverse Recovery Time[4]	t_{rr}	I_S=25A, V_{GS}=0V, V_R=20V, dI_F/dt=100A/us	-	48	-	nS
Reverse Recovery Charge[4]	Q_{rr}		-	46	-	nC

Notes:
1. L=0.1mH, V_{DD}=32V, R_G=25Ω, starting temperature T_J=25°C.
2. Pulse time of 5μs.
3. The dissipated power value will change with the temperature. When it is greater than 25°C, the dissipated power value will decrease by 0.55°C/W for every 1 degree of temperature increase.
4. Pulse test: Pulse width ≤ 300μs, duty cycle ≤ 2%.
5. Basically unaffected by operating temperature.

Typical Electrical and Thermal Characteristic Curves

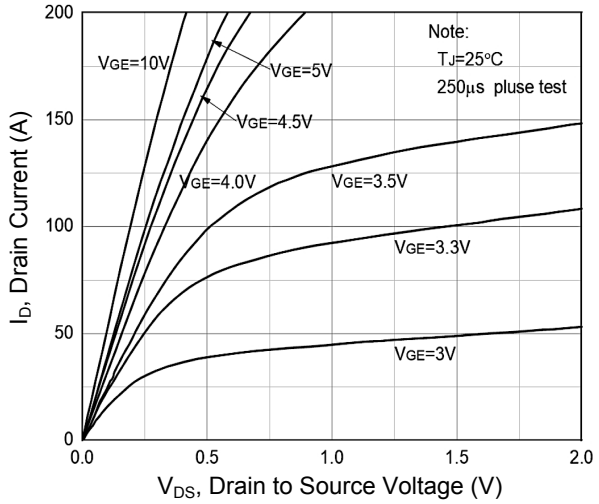


Figure 1. Typical Output Characteristics

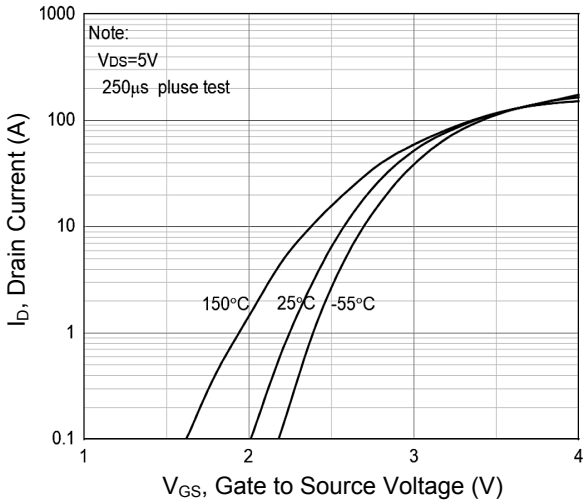


Figure 2. Transfer Characteristics

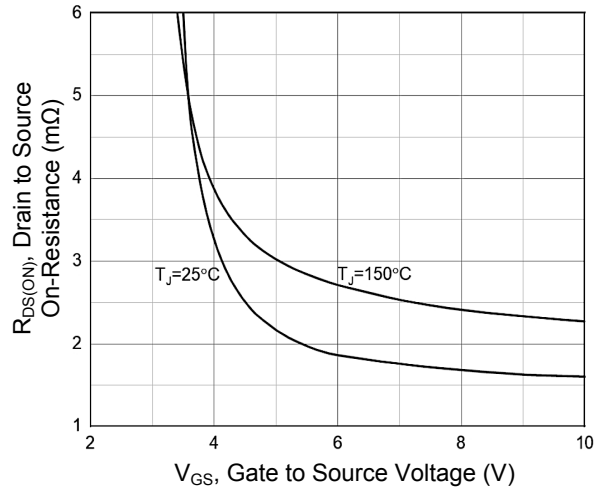


Figure 3. $R_{DS(ON)}$ vs. V_{GS}

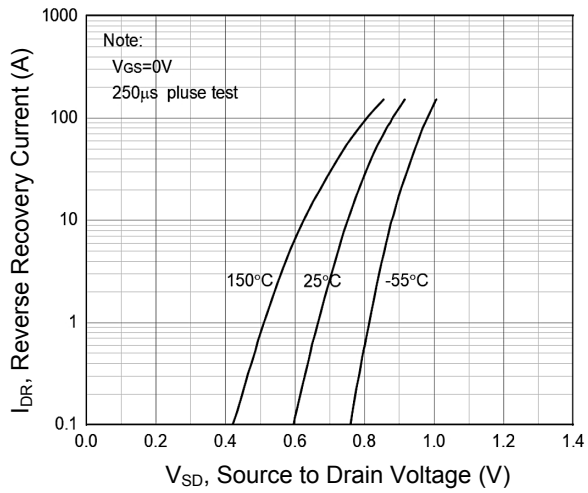


Figure 4. Body Diode Characteristics

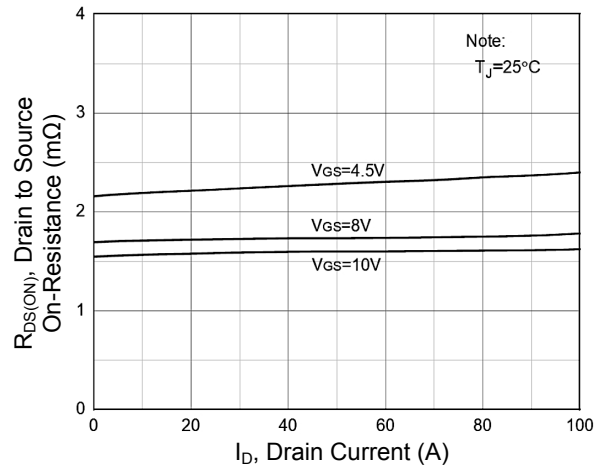


Figure 5. $R_{DS(ON)}$ vs. Drain Current

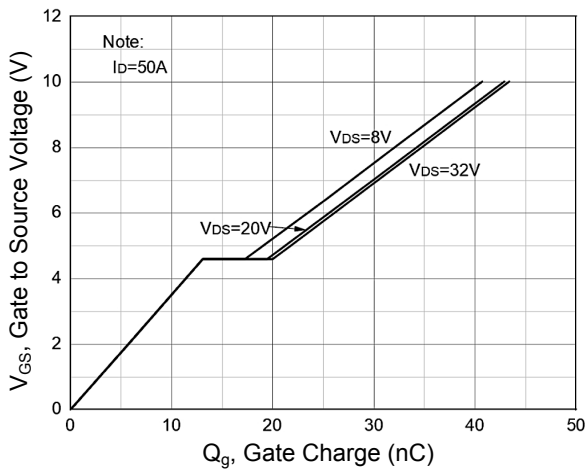


Figure 6. Gate Charge Characteristics

Typical Electrical and Thermal Characteristic Curves

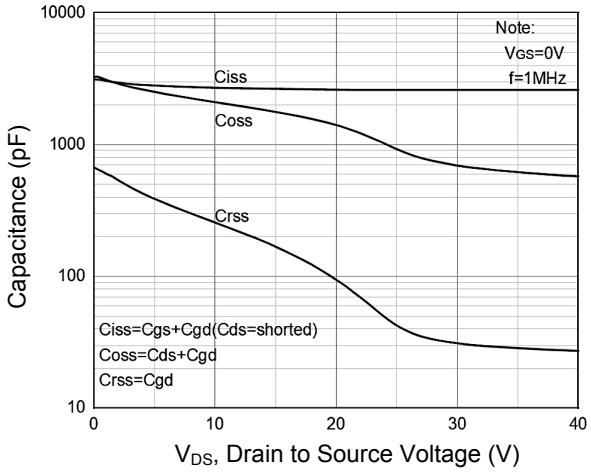


Figure 7. Capacitance Characteristics

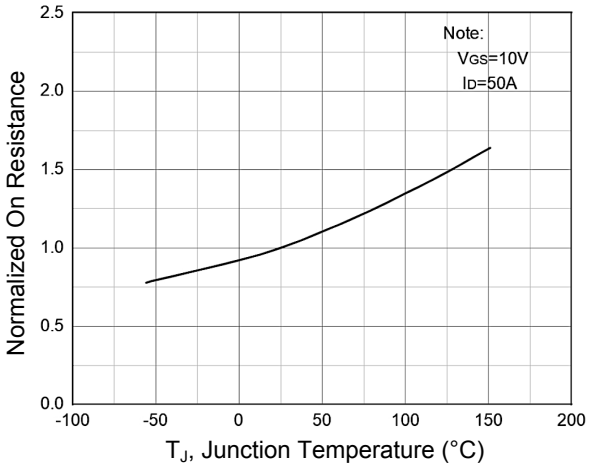


Figure 8. Normalized $R_{DS(ON)}$ vs. T_J

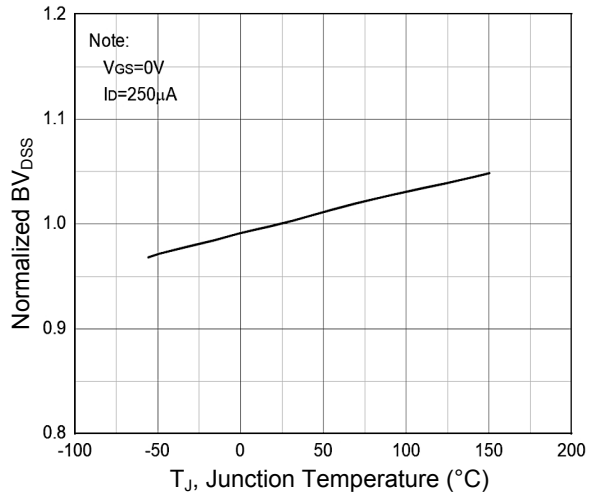


Figure 9. Normalized BV_{DSS} vs. T_J

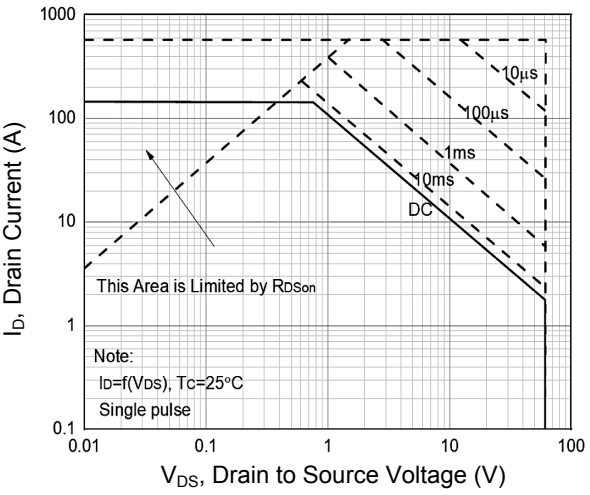


Figure 10. Safe Operation Area

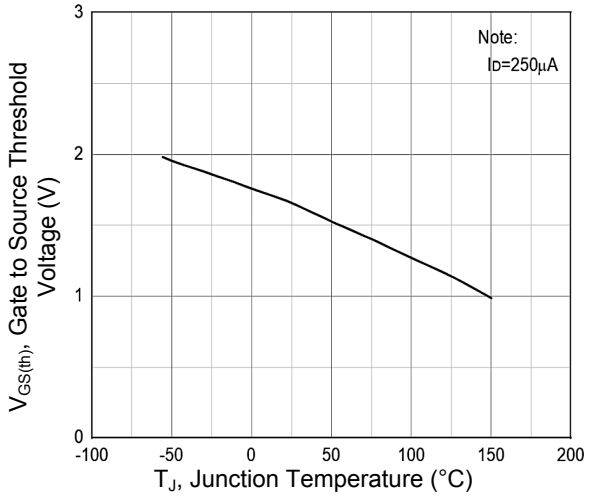
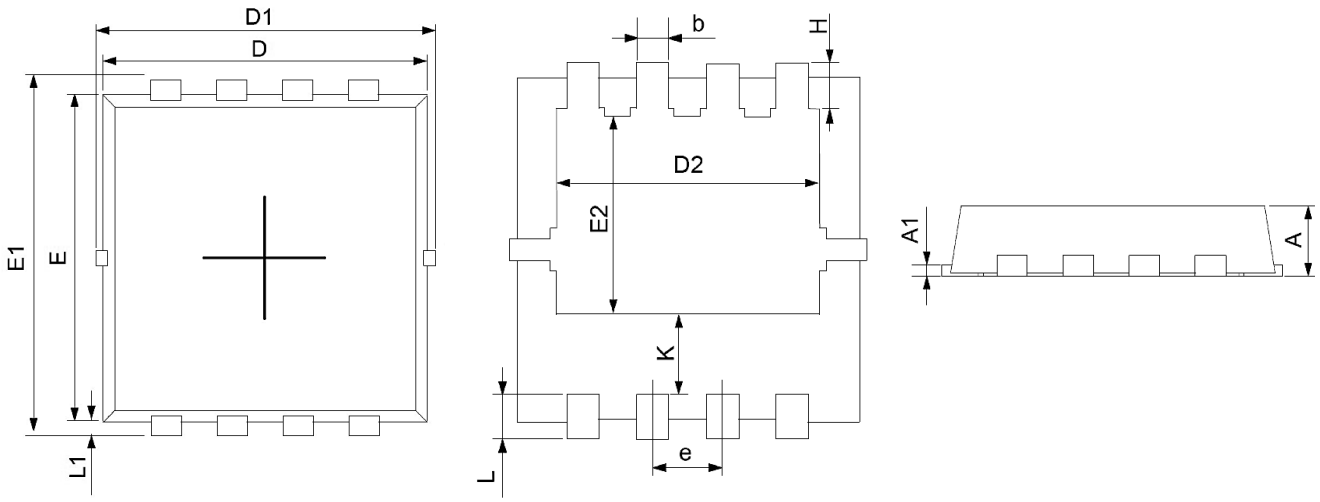


Figure 11. Gate Threshold Voltage vs. T_J

Package Outline Dimensions (PPAK3x3)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.70	0.90	0.028	0.035
A1	0.14	0.20	0.006	0.008
D	3.05	3.25	0.120	0.128
E	2.90	3.10	0.114	0.122
D1	3.10	3.50	0.122	0.138
D2	2.35	2.50	0.093	0.098
E1	3.10	3.50	0.122	0.138
E2	1.64	1.84	0.065	0.072
b	0.25	0.35	0.010	0.014
K	0.59	0.79	0.023	0.031
e	0.55	0.75	0.022	0.030
L	0.25	0.55	0.010	0.022
L1	0.10	0.20	0.004	0.008
H	0.32	0.52	0.013	0.020

Order Information

Device	Package	Marking	Carrier	Quantity
GSGN2R104AU	PPAK3x3	N2R104	Tape & Reel	5,000 Pcs / Reel