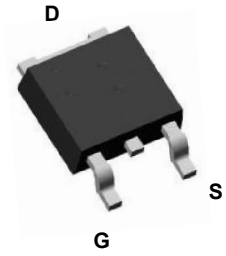
GOOD-ARK SEMICONDUCTOR

GSGD65R400AU

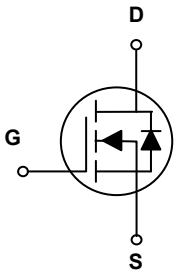
650V N-Channel MOSFET

Main Product Characteristics

$V_{(BR)DSS}$	650V
$R_{DS(ON)}$	0.40Ω (Max.)
I_D	11A



TO-252 (DPAK)



Schematic Diagram

Features and Benefits

- Advanced MOSFET process technology
- Ideal for high efficiency switched mode power supplies
- Low on-resistance with low gate charge
- Fast switching and reverse body recovery
- AEC-Q101 qualified

Description

The GSGD65R400AU utilizes the latest techniques to achieve high cell density and low on-resistance. These features make this device extremely efficient and reliable for use in high efficiency switch mode power supplies and a wide variety of other applications.

Absolute Maximum Ratings (T_A=25°C unless otherwise specified)

Parameter	Symbol	Max.	Unit
Drain-Source Voltage	V_{DS}	650	V
Gate-to-Source Voltage	V_{GS}	±30	V
Continuous Drain Current, @ Steady-State (T_C=25°C)	I_D	11	A
Continuous Drain Current, @ Steady-State (T_C=100°C)		7	A
Pulsed Drain Current	I_{DM}	44	A
Power Dissipation (T_C=25°C)	P_D	96	W
		0.77	W/°C
Single Pulse Avalanche Energy[1]	E_{AS}	356	mJ
Single Pulse Avalanche Current	I_{AS}	2.8	A
Body Diode Reverse Voltage Slope[2]	dv/dt	15	V/ns
MOS dv/dt Ruggedness[3]	dv/dt	100	V/ns
Thermal Resistance, Junction-to-Ambient (PCB Mounted, Steady-State)	$R_{\theta JA}$	62.5	°C/W
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	1.3	°C/W
Operating Junction and Storage Temperature Range	T_J/T_{STG}	-55 to +150	°C
Soldering Temperature	T_{sold}	260	°C

Electrical Characteristics (T_J=25°C unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
On / Off Characteristics						
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V, I_D=250μA	650	-	-	V
Drain-to-Source Leakage Current	I_{DSS}	V_{DS}=650V, V_{GS}=0V, T_J=25°C	-	-	1.0	μA
		V_{DS}=650V, V_{GS}=0V, T_J=125°C	-	1.5	-	μA
Gate-to-Source Forward Leakage	I_{GSS}	V_{DS}=0V, V_{GS}=30V	-	-	100	nA
		V_{DS}=0V, V_{GS}=-30V	-	-	-100	
Static Drain-to-Source On-Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=5.5A	-	0.33	0.40	Ω
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=250μA	2.0	-	4.0	V
Dynamic and Switching Characteristics						
Input Capacitance	C_{iss}	V_{GS}=0V, V_{DS}=100V, f=1MHz	-	925	-	pF
Output Capacitance	C_{oss}		-	30	-	
Reverse Transfer Capacitance	C_{rss}		-	0.8	-	
Total Gate Charge[4,5]	Q_g	I_D=11A, V_{DD}=520V, V_{GS}=10V	-	30	-	nC
Gate-to-Source Charge[4,5]	Q_{gs}		-	7.8	-	
Gate-to-Drain ("Miller") Charge[4,5]	Q_{gd}		-	15	-	
Gate Plateau[4,5]	$V_{plateau}$		-	6.9	-	V
Turn-On Delay Time[4,5]	$T_{d(on)}$	V_{DD}=325V, V_{GS}=10V, R_G=24Ω, I_D=11A	-	15	-	nS
Rise Time[4,5]	T_r		-	35	-	
Turn-Off Delay Time[4,5]	$T_{d(off)}$		-	65	-	
Fall Time[4,5]	T_f		-	30	-	
Gate Resistance	R_g	f=1MHz	-	3.6	-	Ω
Source-Drain Ratings and Characteristics						
Continuous Source Current (Body Diode)	I_S	T_C=25°C, MOSFET symbol showing the integral reverse p-n junction diode.	-	-	11	A
Diode Pulse Current	$I_{S,pulse}$		-	-	44	A
Diode Forward Voltage	V_{SD}	I_S=11A, V_{GS}=0V	-	-	1.4	V
Reverse Recovery Time[4]	t_{rr}	I_S=11A, V_{GS}=0V, dI_F/dt=100A/us	-	254	-	nS
Reverse Recovery Charge[4]	Q_{rr}		-	3.2	-	μC
Reverse Recovery Peak Current[4]	I_{rrm}		-	25	-	A

Notes:

1. L=79mH, V_{DD}=100V, R_G=25Ω, starting temperature T_J=25°C.
2. V_{DS}=0-400V, $I_{SD} \leq I_S$, T_J=25°C.
3. V_{DS}=0-480V.
4. Pulse test: Pulse width ≤ 300us, duty cycle ≤ 2%.
5. Essentially independent of operating Temperature.

Typical Electrical and Thermal Characteristic Curves

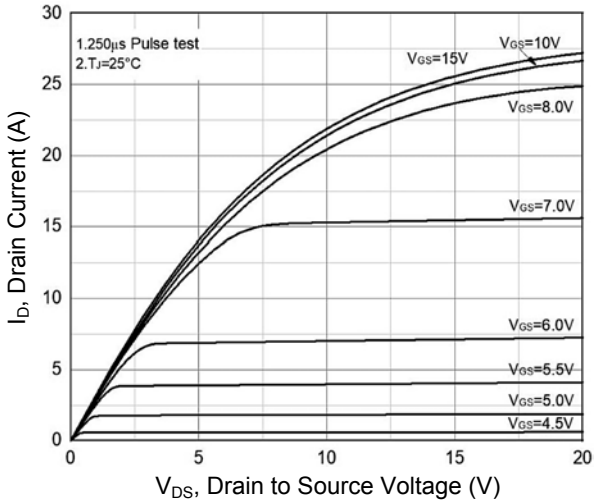


Figure 1. Typical Output Characteristics

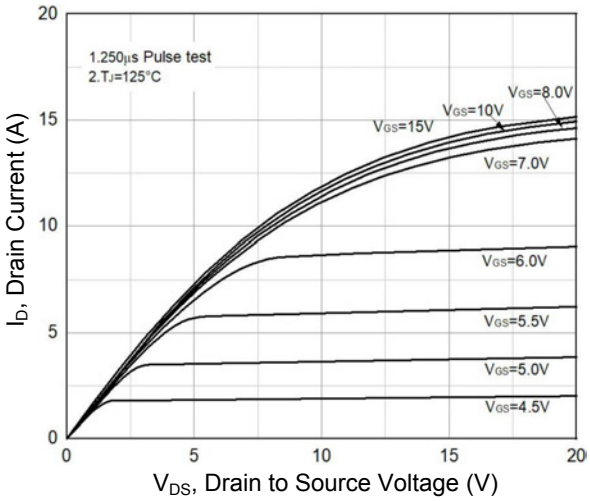


Figure 2. Typical Output Characteristics

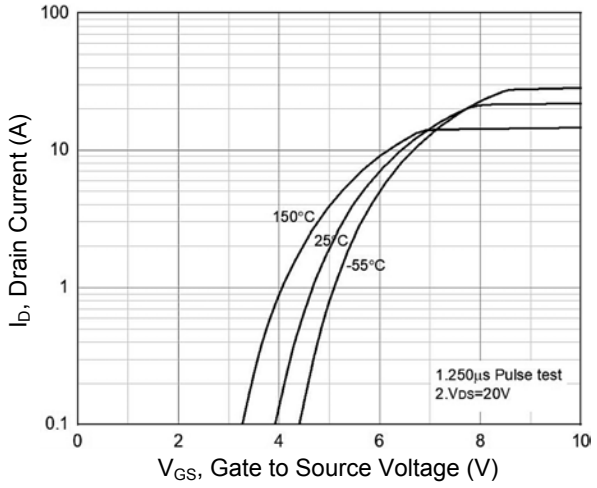


Figure 3. Transfer Characteristics

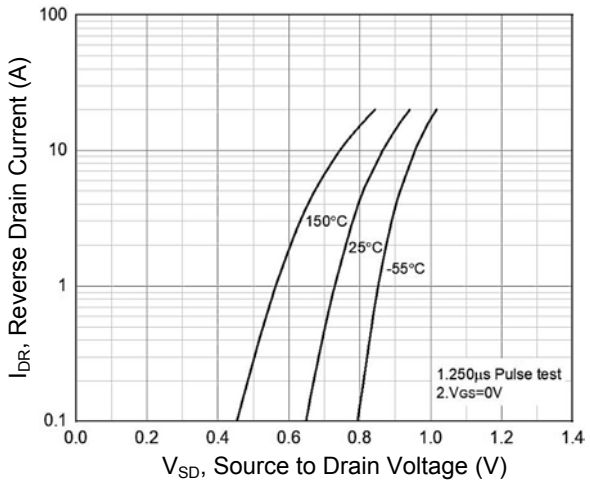


Figure 4. Body Diode Characteristic

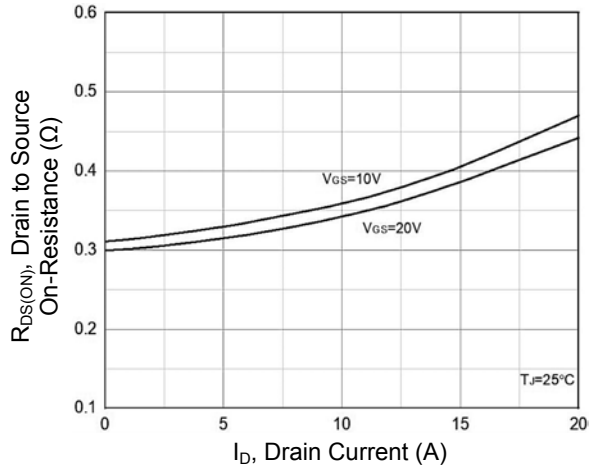


Figure 5. $R_{DS(ON)}$ vs. Drain Current

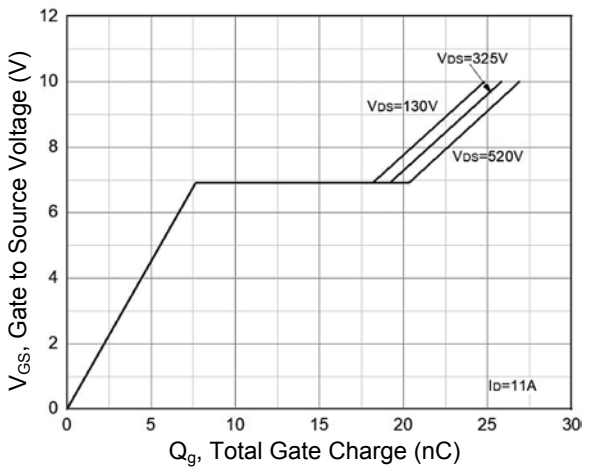


Figure 6. Gate Charge Characteristic

Typical Electrical and Thermal Characteristic Curves

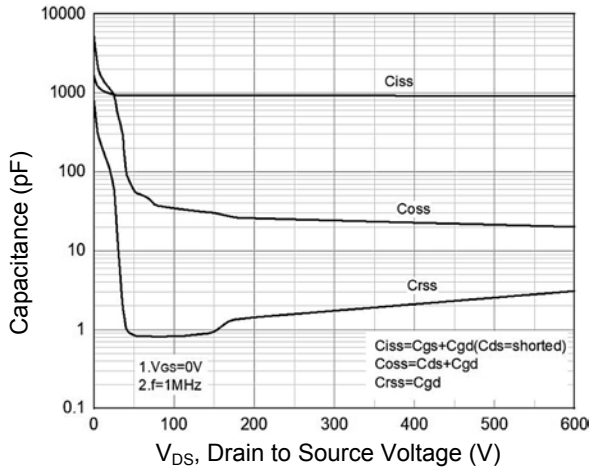


Figure 7. Capacitance Characteristic

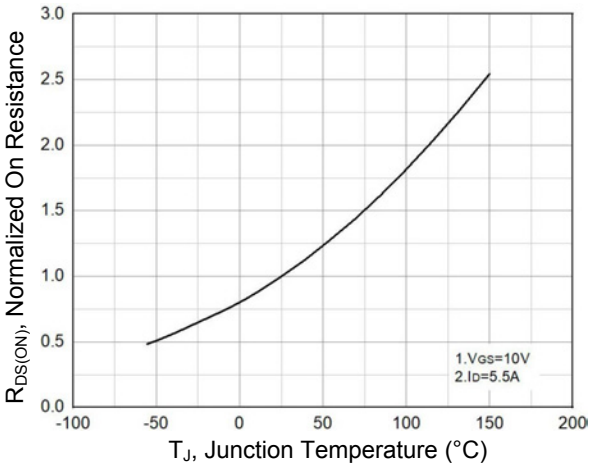


Figure 8. Normalized $R_{DS(ON)}$ vs. T_J

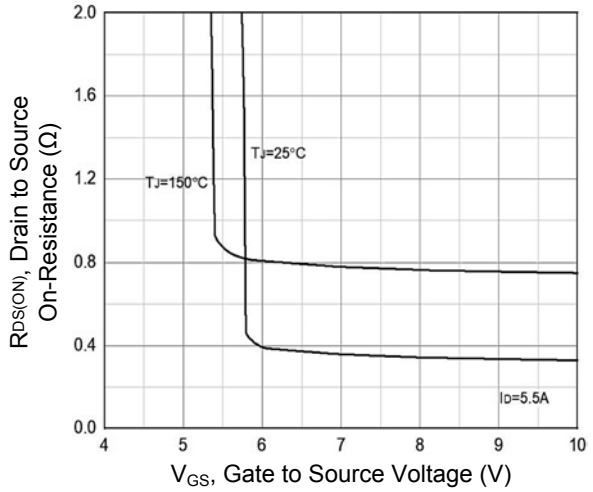


Figure 9. $R_{DS(ON)}$ vs. V_{GS}

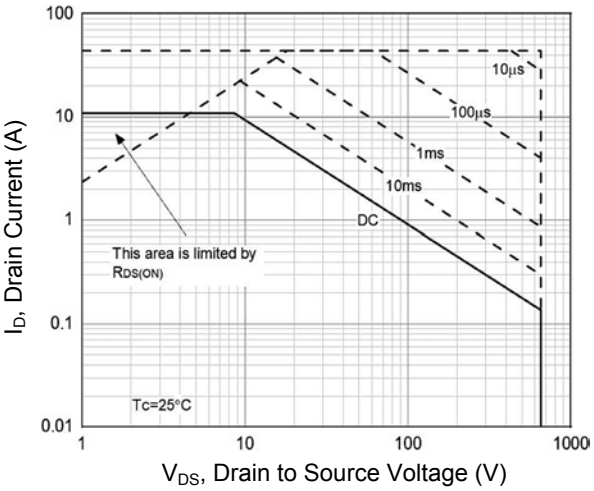


Figure 10. Safe Operation Area

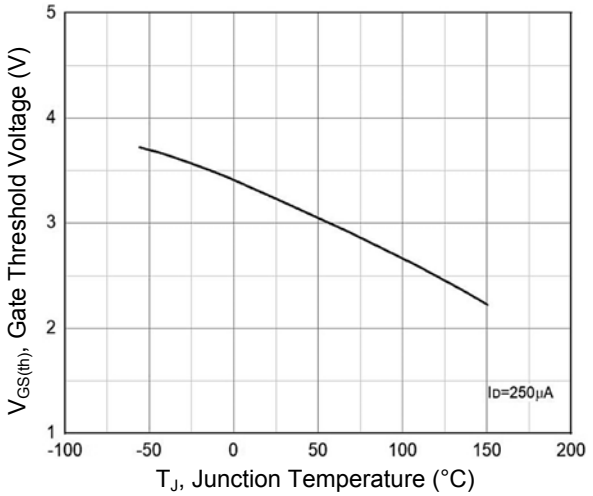


Figure 11. Gate Threshold Voltage vs. T_J

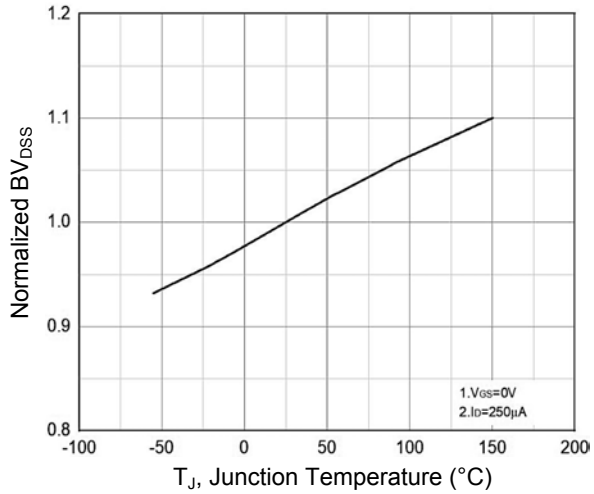
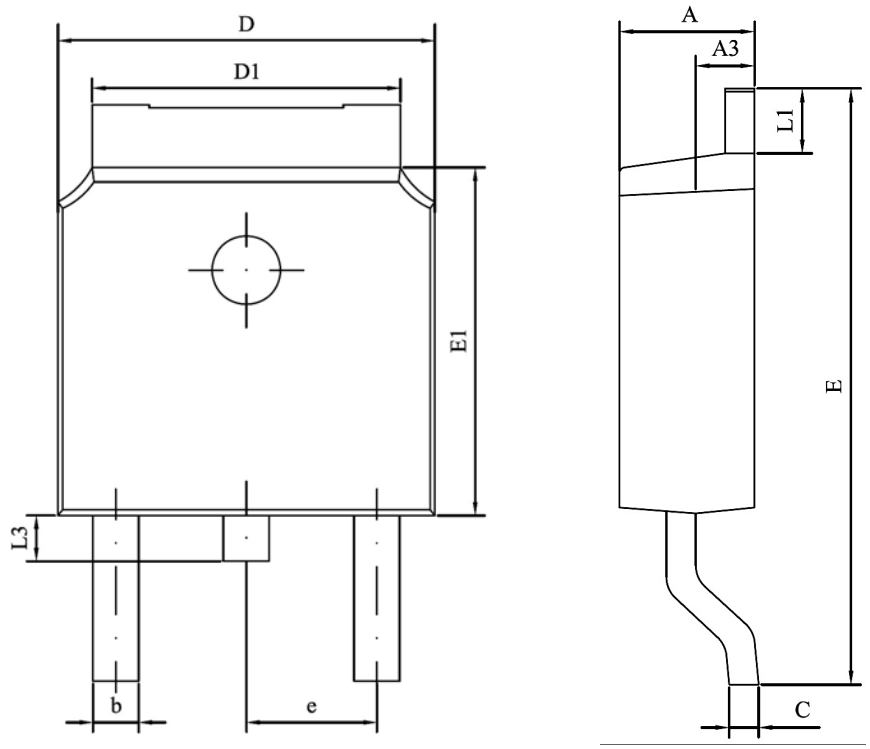


Figure 12. Normalized BV_{DSS} vs. T_J

Package Outline Dimensions TO-252 (DPAK)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	2.150	2.400	0.085	0.094
A3	0.900	1.100	0.035	0.043
b	0.500	0.900	0.020	0.035
C	0.400	0.650	0.016	0.026
D	6.300	6.900	0.248	0.272
D1	4.950	5.500	0.195	0.217
E	9.400	10.410	0.370	0.410
E1	5.900	6.300	0.232	0.248
e	2.286 BSC		0.090 BSC	
L1	0.890	1.270	0.035	0.050
L3	0.600	1.100	0.024	0.043

Order Information

Device	Package	Marking	Carrier	Quantity
GSGD65R400AU	TO-252 (DPAK)	D65R400	Tape & Reel	2,500 Pcs / Reel