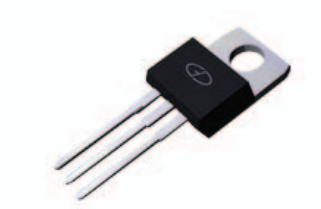
GOOD-ARK SEMICONDUCTOR

SSF180N10P

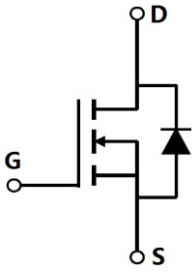
100V N-Channel MOSFET

Main Product Characteristics

V_{DS}	100V
R_{DS}(on)	3mΩ (max.)
I_D	180A



TO-220



Schematic Diagram

Features and Benefits

- Advanced MOSFET process technology
- Ideal for PWM, load switching and general purpose applications
- Ultra low on-resistance with low gate charge
- Fast switching and reverse body recovery
- 100% avalanche rated

RoHS Compliant

Description

The SSF180N10P utilizes the latest trench techniques to achieve high cell density, low on-resistance and high repetitive avalanche rating. These features make this device extremely efficient and reliable for use in power switching applications and a wide variety of other applications.

Absolute Maximum Ratings (T_J=25°C unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain Source Voltage	V_{DS}	100	V
Gate Source Voltage	V_{GS}	±20	V
Continuous Drain Current[1)]	I_D	180	A
Pulsed Drain Current[2)]	$I_{D,\ pulse}$	540	A
Power Dissipation[3)]	P_D	350	W
Single Pulsed Avalanche Energy[5)]	E_{AS}	1000	mJ
Operation and Storage Temperature	T_{STG} , T_J	-55 to 150	℃

Thermal Characteristics

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-Case	RθJC	0.36	℃/W
Thermal Resistance, Junction-Ambient[4)]	RθJA	62.5	℃/W

Electrical Characteristics (T_J=25°C unless otherwise noted)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test condition
Drain-Source Breakdown Voltage	BV_{DSS}	100			V	V_{GS}=0 V, I_D=250 μA
Gate Threshold Voltage	$V_{GS(th)}$	2.0		4.0	V	V_{DS}=V_{GS}, I_D=250 μA
Drain-Source On-State Resistance	$R_{DS(ON)}$		2.5	3.0	mΩ	V_{GS}=10 V, I_D=20 A
Gate-Source Leakage Current	I_{GSS}			100	nA	V_{GS}=20 V
				-100		V_{GS}=-20 V
Drain-Source Leakage Current	I_{DSS}			1	μA	V_{DS}=100 V, V_{GS}=0 V

Dynamic Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test condition
Input Capacitance	C_{iss}		10952.7		pF	V_{GS}=0 V, V_{DS}=50 V, f=100 kHz
Output Capacitance	C_{oss}		1402.2		pF	
Reverse Transfer Capacitance	C_{rss}		33.3		pF	
Turn-on Delay Time	$t_{d(on)}$		40.7		ns	V_{GS}=10 V, V_{DS}=50 V, R_G=2.2 Ω, I_D=25 A
Rise Time	t_r		31.4		ns	
Turn-Off Delay Time	$t_{d(off)}$		75.4		ns	
Fall Time	t_f		16.2		ns	

Gate Charge Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test condition
Total Gate Charge	Q_g		158.8		nC	I_D=25 A, V_{DS}=50 V, V_{GS}=10 V
Gate-Source Charge	Q_{gs}		38.4		nC	
Gate-Drain Charge	Q_{gd}		41.6		nC	
Gate Plateau Voltage	$V_{plateau}$		4.6		V	

Body Diode Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test condition
Diode Forward Current	I_S			180	A	V_{GS}<V_{th}
Pulsed Source Current	I_{SP}			540		
Diode Forward Voltage	V_{SD}			1.3	V	I_S=20 A, V_{GS}=0 V
Reverse Recovery Time	t_{rr}		99.2		ns	I_S=25 A, di/dt=100 A/μs
Reverse Recovery Charge	Q_{rr}		401.9		nC	
Peak Reverse Recovery Current	I_{rrm}		6.7		A	

Notes:

1) Calculated continuous current based on maximum allowable junction temperature.
2) Repetitive rating; pulse width limited by max. junction temperature.
3) Pd is based on max. junction temperature, using junction-case thermal resistance.
4) The value of $R_{\theta JA}$ is measured with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with T_a=25 ℃.
5) V_{DD}=50 V, R_G=25 Ω, L=0.3 mH, starting T_J=25 ℃.

Typical Characteristic Curves

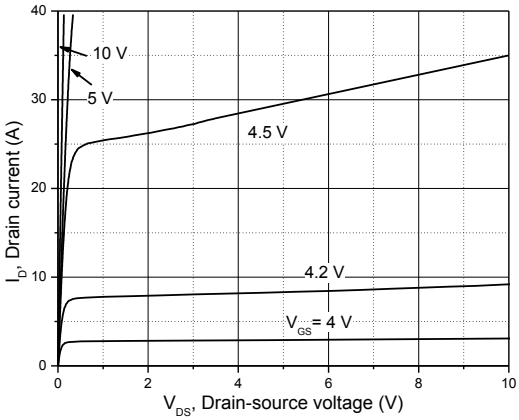


Figure 1, Typ. output characteristics

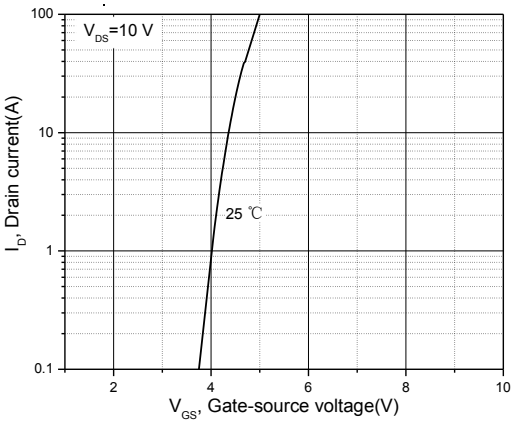


Figure 2, Typ. transfer characteristics

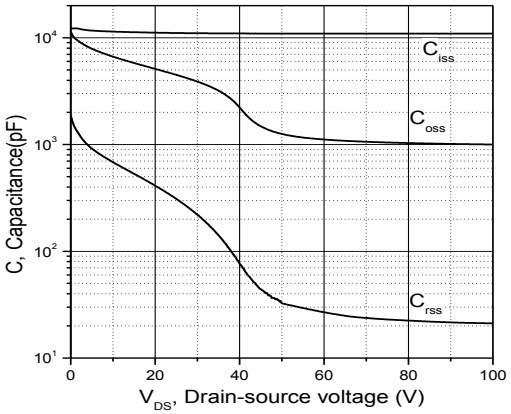


Figure 3, Typ. capacitances

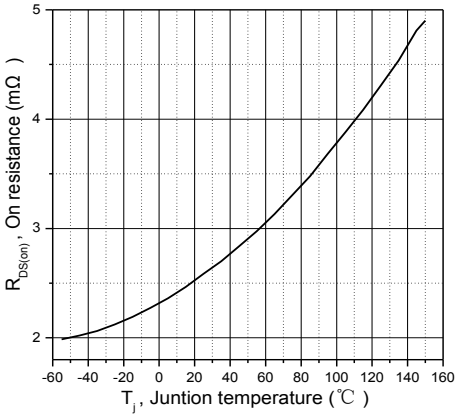


Figure 4, Typ. gate charge

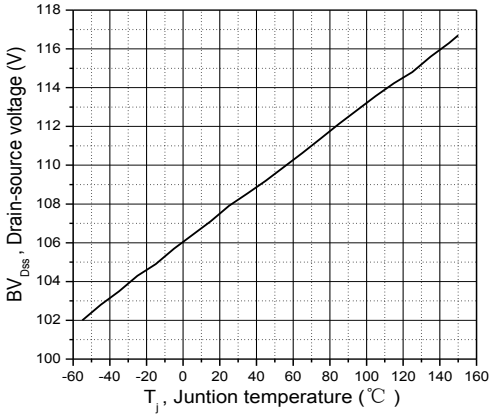


Figure 5, Drain-source breakdown voltage

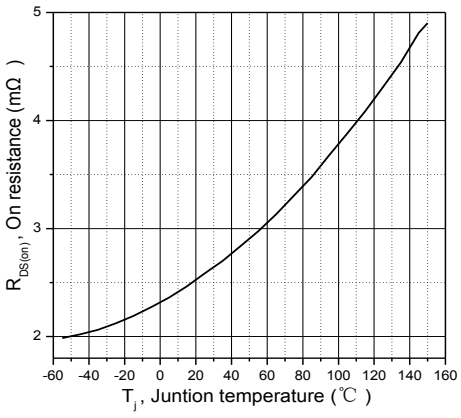


Figure 6, Drain-source on-state resistance

Typical Characteristic Curves

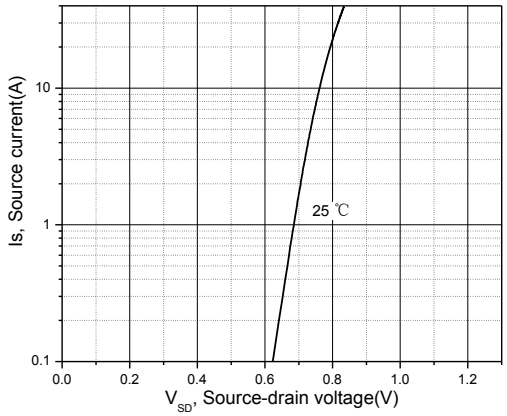


Figure 7, Forward characteristic of body diode

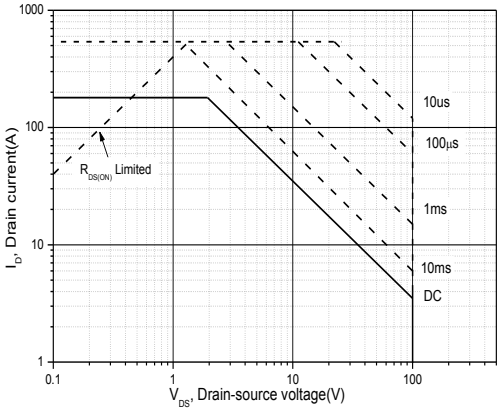


Figure 8, Safe operation area T_C=25 ℃

Test Circuits and Waveforms

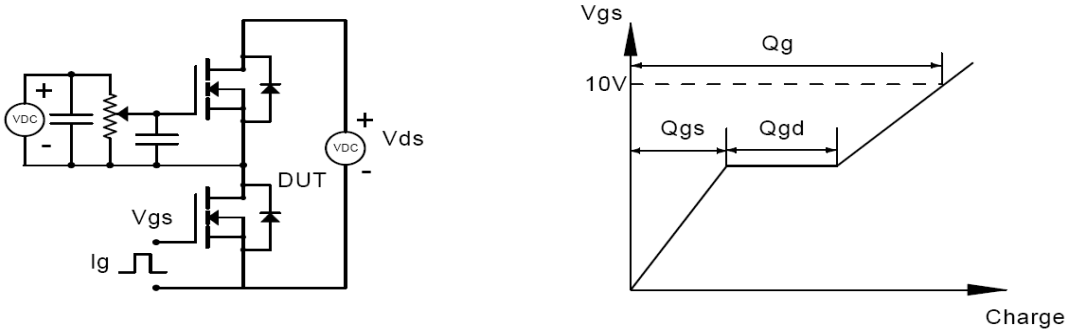


Figure 1, Gate charge test circuit & waveform

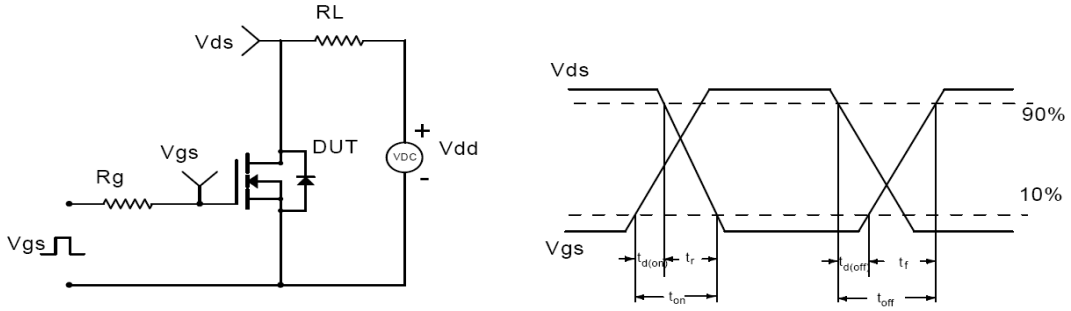


Figure 2, Switching time test circuit & waveforms

Test Circuits and Waveforms

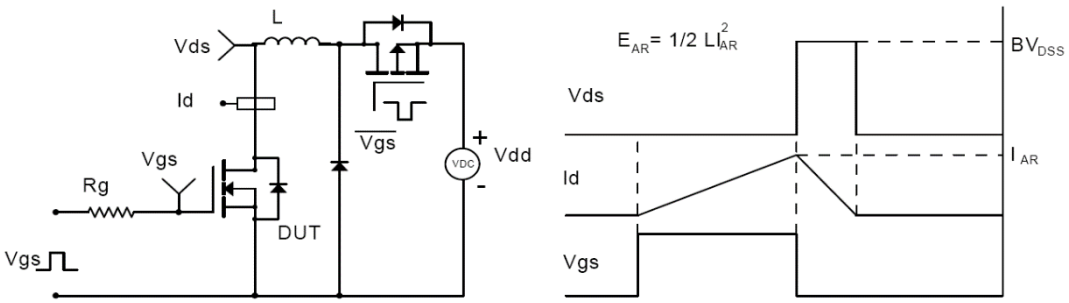


Figure 3, Unclamped inductive switching (UIS) test circuit & waveforms

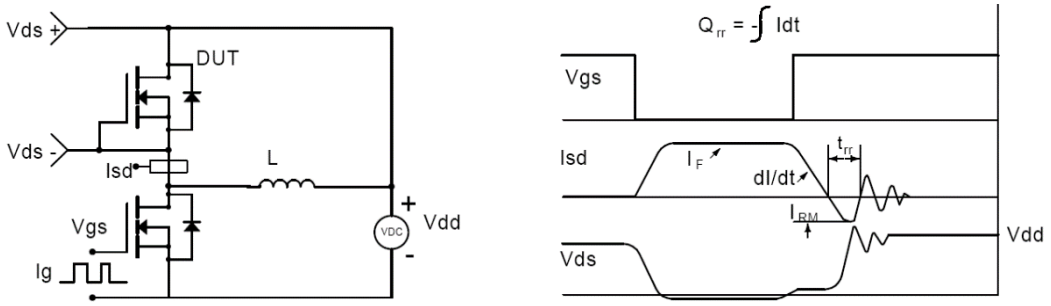
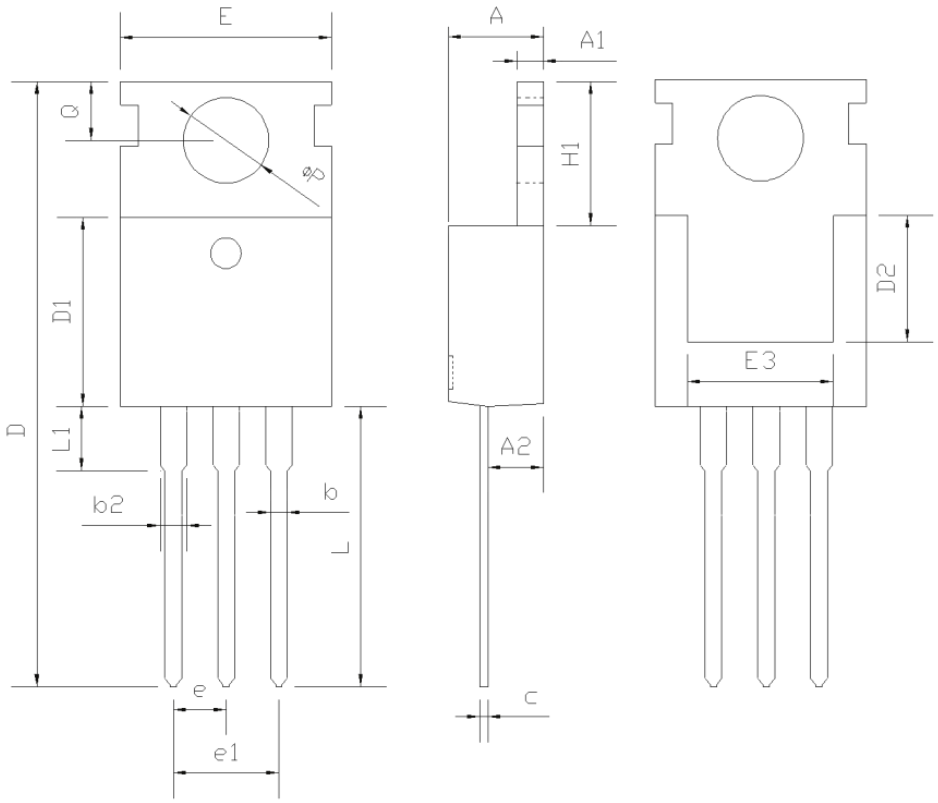


Figure 4, Diode reverse recovery test circuit & waveforms

Package Outline Dimensions TO-220



Symbol	Min	Nom	Max
A	4.37	4.57	4.77
A1	1.25	1.30	1.45
A2	2.20	2.40	2.60
b	0.70	0.80	0.95
b2	1.17	1.27	1.47
c	0.40	0.50	0.65
D	15.10	15.60	16.10
D1	8.80	9.10	9.40
D2	5.50	-	-
E	9.70	10.00	10.30
E3	7.00	-	-
e	2.54 BSC		
e1	5.08 BSC		
H1	6.25	6.50	6.85
L	12.75	13.50	13.80
L1	-	3.10	3.40
ΦP	3.40	3.60	3.80
Q	2.60	2.80	3.00