GOOD-ARK SEMICONDUCTOR

SSF11NS65UD

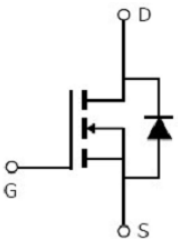
650V N-Channel MOSFET

Main Product Characteristics

V_{DSS}	650V
$R_{DS(on)}$	0.33Ω (typ.)
I_D	11A

TO-252 (DPAK)

Marking and Pin Assignment



Schematic Diagram

Features and Benefits

- High dv/dt and avalanche capabilities
- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance

Description

The SSF11NS65UD utilizes the latest processing techniques to achieve high cell density, low on-resistance and high repetitive avalanche rating. These features make this device extremely efficient and reliable for use in power switching applications and a wide variety of other applications.

Absolute Maximum Ratings

Symbol	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V①	11	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V①	7	
I_{DM}	Pulsed Drain Current②	44	
P_D @T_C = 25°C	Power Dissipation③	49	W
	Linear Derating Factor	0.4	W/°C
V_{DS}	Drain-Source Voltage	650	V
V_{GS}	Gate-to-Source Voltage	± 30	V
E_{AS}	Single Pulse Avalanche Energy @ L=129.6mH	305	mJ
I_{AS}	Avalanche Current @ L=129.6mH	2.17	A
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +150	℃

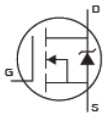
Thermal Resistance

Symbol	Characteristics	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case③	—	2.53	°C/W
$R_{\theta JA}$	Junction-to-Ambient (t ≤ 10s) ④	—	62	°C/W

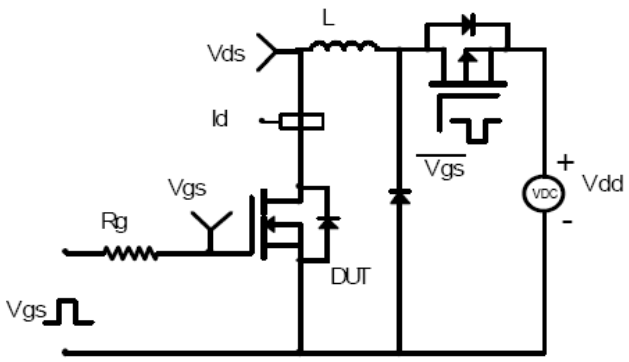
Electrical Characteristics (T_A=25°C unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	650	—	—	V	V_{GS} = 0V, I_D = 250μA
$R_{DS(on)}$	Static Drain-to-Source On-resistance	—	0.33	0.38	Ω	V_{GS}=10V, I_D = 5.5A
		—	0.74	—		T_J = 125℃
$V_{GS(th)}$	Gate Threshold Voltage	2	—	4	V	V_{DS} = V_{GS}, I_D = 250μA
		—	2.1	—		T_J = 125℃
I_{DSS}	Drain-to-Source Leakage Current	—	—	1	μA	V_{DS} =650V, V_{GS} = 0V
		—	—	50		T_J = 125℃
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V_{GS} =30V
		—	—	-100		V_{GS} = -30V
Q_g	Total Gate Charge	—	22	—	nC	I_D= 4.8A, V_{DS}= 480V, V_{GS} = 10V
Q_{gs}	Gate-to-Source Charge	—	4.3	—		
Q_{gd}	Gate-to-Drain("Miller") Charge	—	8	—		
$t_{d(on)}$	Turn-on Delay Time	—	11	—	ns	V_{GS}=10V, V_{DS}=400V, R_L=81.6Ω, R_{GEN}=3.4Ω I_D=4.9A
t_r	Rise Time	—	6	—		
$t_{d(off)}$	Turn-Off Delay Time	—	29	—		
t_f	Fall Time	—	6	—		
C_{iss}	Input Capacitance	—	808	—	pF	V_{GS} = 0V V_{DS} = 100V f = 1MHz
C_{oss}	Output Capacitance	—	34	—		
C_{rss}	Reverse Transfer Capacitance	—	3.1	—		

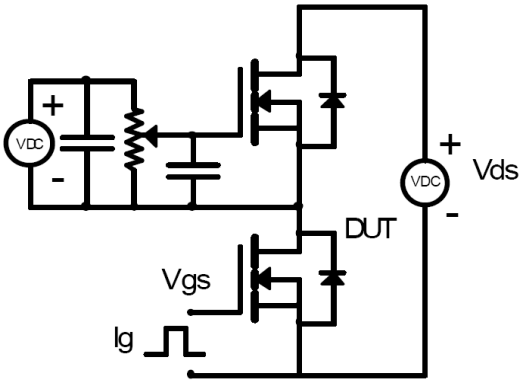
Source-Drain Ratings and Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	11	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode)	—	—	44	A	
V_{sd}	Diode Forward Voltage	—	0.82	1.2	V	I_S=5.5A, V_{GS}=0V
t_{rr}	Reverse Recovery Time	—	247	—	ns	T_J = 25°C, I_F =4.8A, di/dt = 100A/μs
Q_{rr}	Reverse Recovery Charge	—	2.4	—	μC	

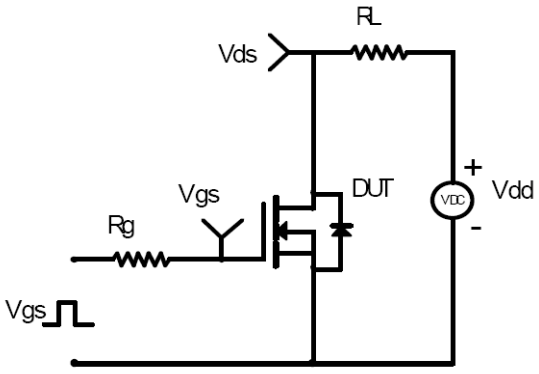
Test Circuits and Waveforms



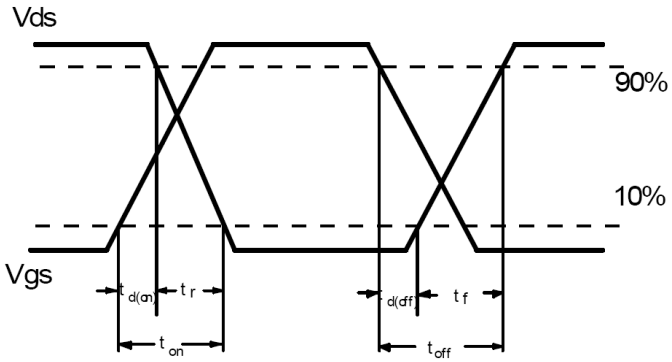
E_{AS} Test Circuit



Gate Charge Test Circuit



Switching Time Test Circuit



Switching Waveforms

Notes:

①Calculated continuous current based on maximum allowable junction temperature.

②Repetitive rating; pulse width limited by max. junction temperature.

③The power dissipation P_D is based on max. junction temperature, using junction-to-case thermal resistance.

④The value of $R_{\theta JA}$ is measured with the device mounted on 1 in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A =25°C

Typical Electrical and Thermal Characteristics

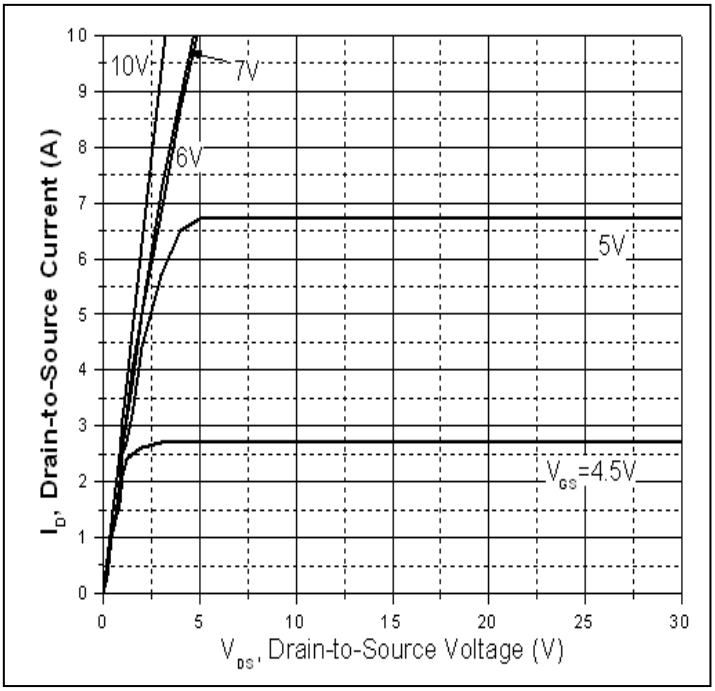


Figure 1. Typical Output Characteristics

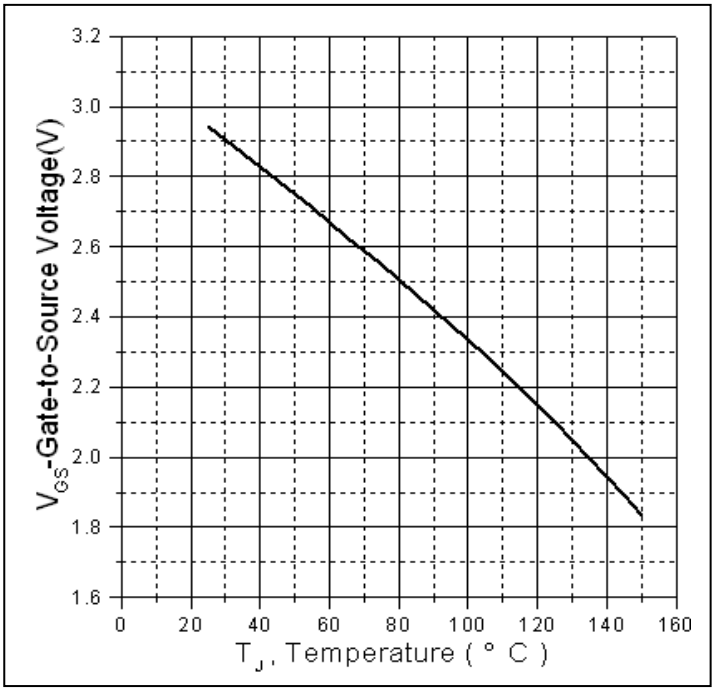


Figure 2. Gate to Source Cut-off Voltage

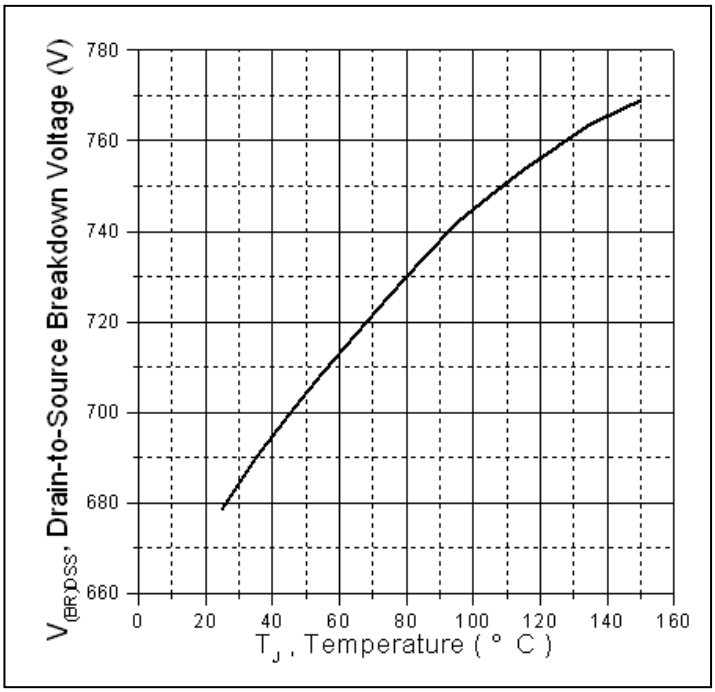


Figure 3. Drain-to-Source Breakdown Voltage Vs. Case Temperature

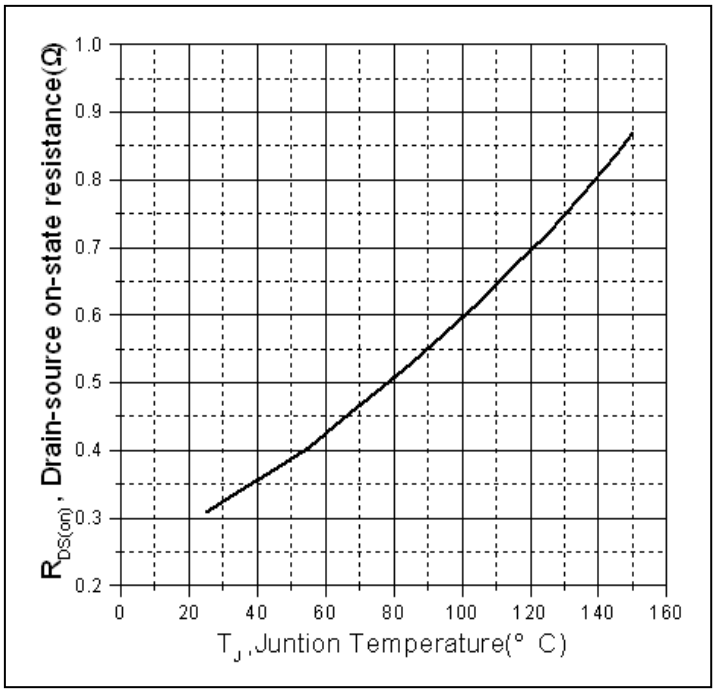


Figure 4. Normalized On-Resistance Vs. Case Temperature

Typical Electrical and Thermal Characteristics

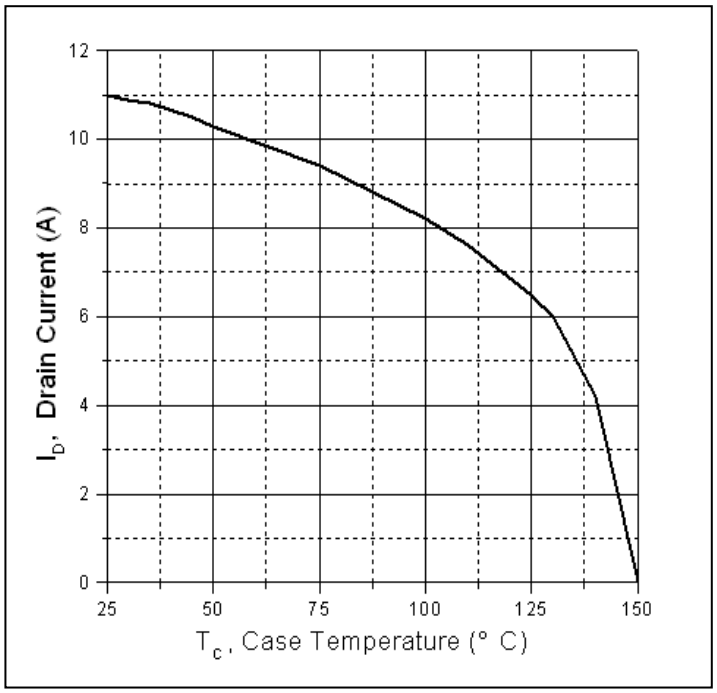


Figure 5. Maximum Drain Current Vs. Case Temperature

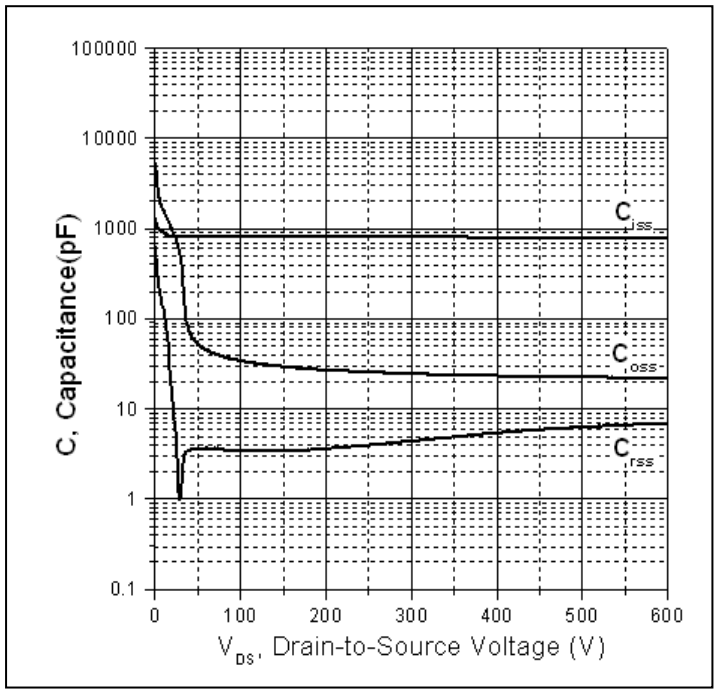


Figure 6. Typical Capacitance Vs. Drain-to-Source Voltage

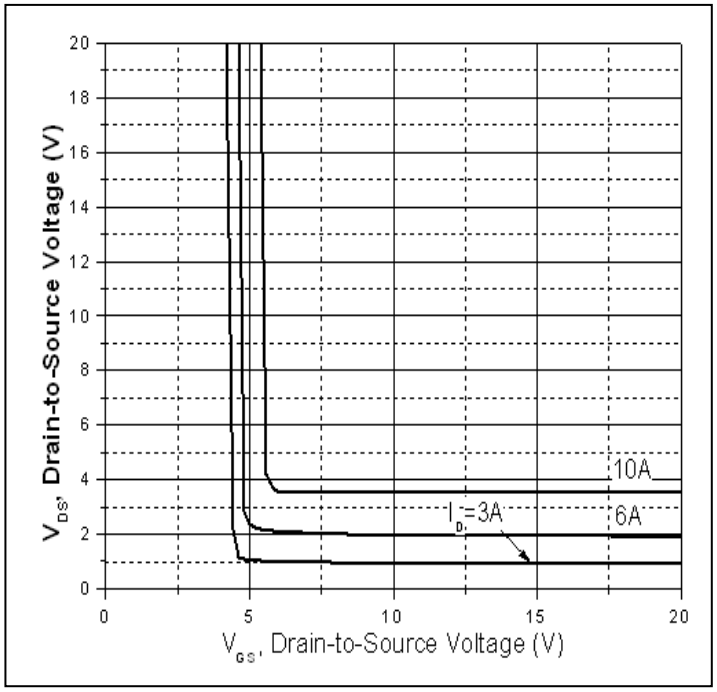


Figure 7. Drain-to-Source Voltage Vs. Gate-to-Source Voltage

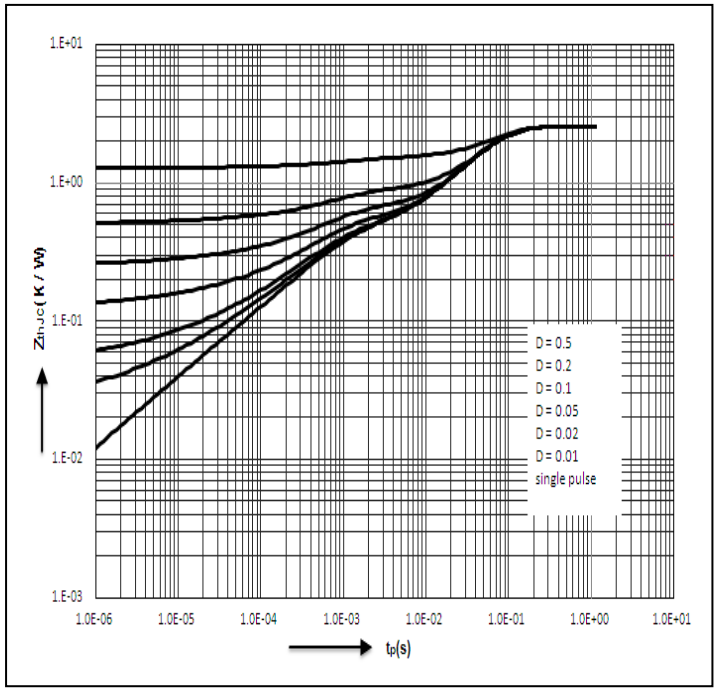
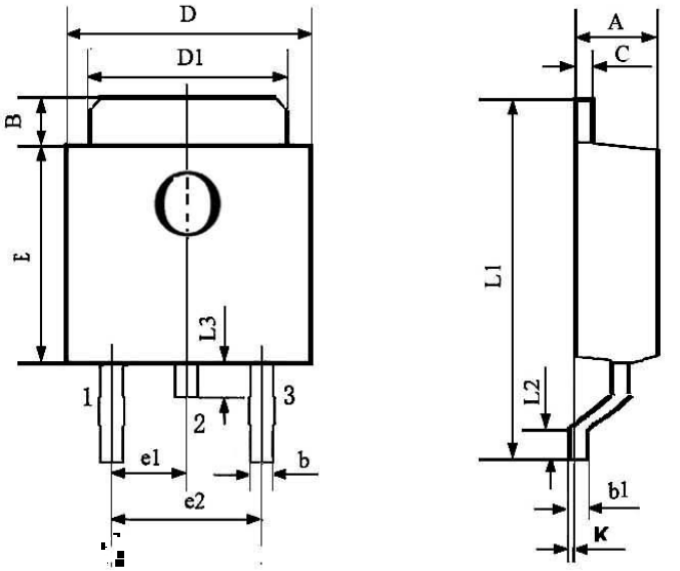


Figure 8. Maximum Effective Transient Thermal Impedance, Junction-to-Case

Mechanical Data

TO-252/DPAK PACKAGE OUTLINE DIMENSION



Symbol	Dimensions In Millimeters			Dimensions In Inches		
	Min	Nom	Max	Min	Nom	Max
A	2.200	-	2.400	0.087	-	0.094
B	0.950	-	1.250	0.037	-	0.049
b	0.500	-	0.700	0.020	-	0.028
b1	0.450	-	0.550	0.018	-	0.022
C	0.450	-	0.550	0.018	-	0.022
D	6.450	-	6.750	0.254	-	0.266
D1	5.200	-	5.400	0.205	-	0.213
E	5.950	-	6.250	0.234	-	0.246
e1	2.240	-	2.340	0.088	-	0.092
e2	4.430	-	4.730	0.174	-	0.186
L1	9.450	-	9.950	0.372	-	0.392
L2	1.250	-	1.750	0.049	-	0.069
L3	0.600	-	0.900	0.024	-	0.035
K	0.000	-	0.100	0.000	-	0.004

Ordering and Marking Information

Device Marking: SSF11NS65UD

Package (Available)

TO-252/DPAK

Operating Temperature Range

C: -55 to 150°C

Devices per Unit（Options）

Package Type	Units/Tape	Tapes/Inner Box	Units/Inner Box	Inner Boxes/ Carton Box	Units/ Carton Box
TO-252	2500	2	5000	7	35000
TO-252	2500	1	2500	10	25000
TO-252	800	5	4000	8	32000

Reliability Test Program

Test Item	Conditions	Duration	Sample Size
High Temperature Reverse Bias(HTRB)	T_j=125°C to 150°C @ 80% of Max $V_{DSS}/V_{CES}/V_R$	168 hours 500 hours 1000 hours	3 lots x 77 devices
High Temperature Gate Bias(HTGB)	T_j=150°C @ 100% of Max V_{GSS}	168 hours 500 hours 1000 hours	3 lots x 77 devices